STUDIES OF SHORT CHANNEL EFFECTS AND PERFORMANCE ENHANCEMENT OF NANO-MOSFET BASED ON MULTI-OBJECTIVE GENETIC ALGORITHM APPROACH

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CERTIFICATE

This is to certify that the thesis entitled **Studies of Short Channel Effects and Performance Enhancement of Nano-MOSFET based on Multi-Objective Genetic Algorithm Approach**, submitted by SARITA PANIGRAHY to National Institute of Technology, Rourkela, is a record of bonafide research work under my supervision and I consider it worthy of consideration for award of the degree of Master of Technology (Research) of the Institute.

Prof. P. K. Sahu
(Supervisor)

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Last but not the least, I am grateful to Almighty for His grace.

Sarita Panigrahy

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DECLARATION

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SARITA PANIGRAHY

Abstract

The nano-scale devices face a major issue i.e Short Channel Effects, as a result of which the performance of the devices degrade. To enhance the performance of such devices, the SCEs should be reduced.

This thesis contributes to enhance the performance of nano-scaled DG MOSFET by reducing the short channel effects. To approach towards the main objective of the thesis, a study has been done on analytical modeling of undoped symmetric DG MOSFET. Then, to get the picture of SCEs, the electrical parameters such as maximum Drain current(I_{on}), Leakage current(I_{off}), Sub threshold Swing (SS), Threshold voltage (V_{th}), and Drain Induced Barrier Lowering (DIBL) are analytically derived by solving 2-dimensional Poisson's equation and the same are studied with the variation of design parameters such as L, t_{si} and t_{ox}. To validate such analytical models, SCEs are studied using ATLAS device simulator. Graded Cannel engineering techniques are used for reduction of SCEs. For further reduction or minimization of SCEs, a multi-objective optimization technique is used to enhance the accuracy with optimum design parameters. To validate the optimized structure, a simulated model is built with those optimized values of the design parameter and the performance of the device is compared with the existing result [32].

Key words: Double Gate Metal Oxide Semiconductor Field Effect Transistor (DG MOSFET), Short Channel Effect (SCE), Graded Channel Engineering (GCE), Multi Objective Genetic Algorithm (MOGA).

Contents

List of Symbols

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ε_{si}	:	Permittivity of silicon,
n_i	:	Intrinsic carrier density,
ψ	:	Electric potential of the device,
K	:	Boltzmann's constant,
T	:	Temperature of the silicon film in Kelvin,
ϕ	:	Work function of the gate material in eV,
ε_{ox}	:	Permittivity of the oxide layer,
t_{ox}	:	Thickness of the oxide layer,
t_{si}	:	Thickness of the silicon layer,
L	:	Length of the channel,
Q_i	:	Charge sheet density of the inversion layer,
N_D	:	Donor concentration,
ϕ_{ms}	:	Gate work function referenced to intrinsic silicon,
h	:	Plank's constant,
E	:	Electric field,
$L_{\min}$	:	Minimum channel length,
W_d	:	Depletion width of Bulk MOSFET,
Q_d	:	Depletion charge sheet density,
Q_i	:	Inversion charge sheet density,
ψ_s	:	Surface potential,

List of Symbols

V_g	:	Gate voltage,
V_d	:	Drain voltage,
V_{th}	:	Threshold voltage,
$V_{thermal}$	:	Thermal voltage,
μ_{eff}	:	Effective mobility,
Q_s	:	Charge at the source end of the channel,
C_{ox}	:	Capacitance of the oxide layer,
C_{si}	:	Capacitance of the silicon layer,
ϕ_i	:	Gate work function,
L_e	:	Effective gate length,
N_A	:	Channel doping concentration,
V_{FB}	:	Flat band voltage,
λ	:	Natural channel length,
V_{bi}	:	Built in potential across the source/drain channel junction ,
Q_{th}	:	Carrier charge density in threshold region,
Q_{inv}	:	Carrier charge density in inversion region,
L_e	:	Effective gate length after the effect of velocity saturation ,
V_{sat}	:	Saturation potential ,
ν_{sat}	:	Velocity saturation.

List of Acronyms

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DIBL	:	Drain Induced Barrier lowering,
SS	:	Sub-threshold Swing,
SCE	:	Short Channel Effect,
I_{off}	:	Leakage Current,
I_{on}	:	Maximum Drain Current,
CE	:	Channel Engineering,
GCE	:	Graded Channel Engineering,
SDDG	:	Simultaneously Driven Double Gate,
IDDG	:	Independently Driven Double Gate,
GA	:	Genetic Algorithm,
MOGA	:	Multi Objective Genetic Algorithm,
ITRS	:	International Technology Road map for Semiconductor,
MOSFET	:	Metal Oxide Semiconductor Field Effect Transistor,
BJT	:	Bipolar Junction Transistor,
1-D	:	One-dimensional,
2-D	:	Two-dimensional,
SOI	:	Silicon-on-Insulator.

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CHAPTER 1

Introduction

The Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) has been the driving engine of the semiconductor industry because of its successful incorporation into the integrated circuits (ICs). CMOS technology evolution in the past few decades has followed the path of device scaling to achieve density, speed and power improvement. As indicated by the Moores law, the number of transistors inside the chips doubles in every two years because of the shrinking size of MOSFETs. It is well known that reducing the source-to-drain spacing, i.e., the channel length of a MOSFET, the driving current in the channel increases. It also leads to the Short Channel Effects (SCEs) in the device. The most undesirable SCE is the reduction in the threshold voltage (V_{th}) at which the device turns on, especially at high drain voltage. The reduced threshold voltage causes the subthreshold leakage current to increase dramatically, which makes the device difficult to turn off. New high-resolution lithographic techniques therefore required for the development of new device designs, technologies, and the structures that can keep the SCEs under control at very small dimensions.

1.1 Past history and future trends of MOSFET scaling

To reduce IC size and improve the performance of the device, transistor size has been rapidly decreasing over the past four decades. The physical size of the device has been scaled down and the number of transistors integrated in a single chip has been doubled in every 24 months [1]. The BJT was invented in 1947. To replace BJT, CMOS was developed, which are smaller in size and faster in speed. The MOSFET has been the most popular semiconductor device since its discovery in 1970s. Still the downscaling procedure continue to fulfill the demand of better performing electronics. The smaller dimension transistors are having better qualities in terms of higher current drive, faster processing speed compared to CMOS. The capabilities of many digital devices are totally dependent on Moore's law. The capabilities include processing speed, memory capacity and packing density. The law is named according to Intel co-founder Gordon E. Moore. He has developed that the number of components in integrated circuits had doubled in every year from the invention of the integrated circuit in 1958 until 1965 and he predicted that the trend will continue for at least 10 years. His prediction is proved to be accurate, because now a days this law is used in the semiconductor industry. This law is used to update the International Technology Road map for semiconductor (ITRS). This law is also used in industries to guide long term planning and set targets for research and development. Moore's law shows the shrinking dimensions on an exponential curve with a number of transistors doubling in every 2 years. By this formula the current chips consists of more than billion of transistors. As the transistor technology continues to advance, the transistor performance progresses. Fig. 1.1 shows the progression of transistor performance with respect to continuous advancement of transistor technology [2].

Scaling is not limited to the reduction in the gate length of the transistors but also involves scaling down the thickness of the oxide layers, voltage applied to device and change in doping concentration of the substrate [3]. The factor by which these parameters are changed is called as the scaling factor (α). The scaling concept is schematically illustrated in Fig. 1.2, in which the device dimensions and device voltages are scaled down and the doping concentration is scaled up by the same factor. Then, according to basic electrostatics, the electric field configuration will be same as the original device. A larger MOSFET can then be scaled down to a smaller MOSFET with similar behavior. The scaling rules for MOSFET devices and circuit parameters are shown in Table 1.1. These scaling rules only give us a guideline to shrink down a device. They do not tell us how small we can make the devices. For a given supply voltage and given layer thickness, as the channel length decreases, the MOSFET

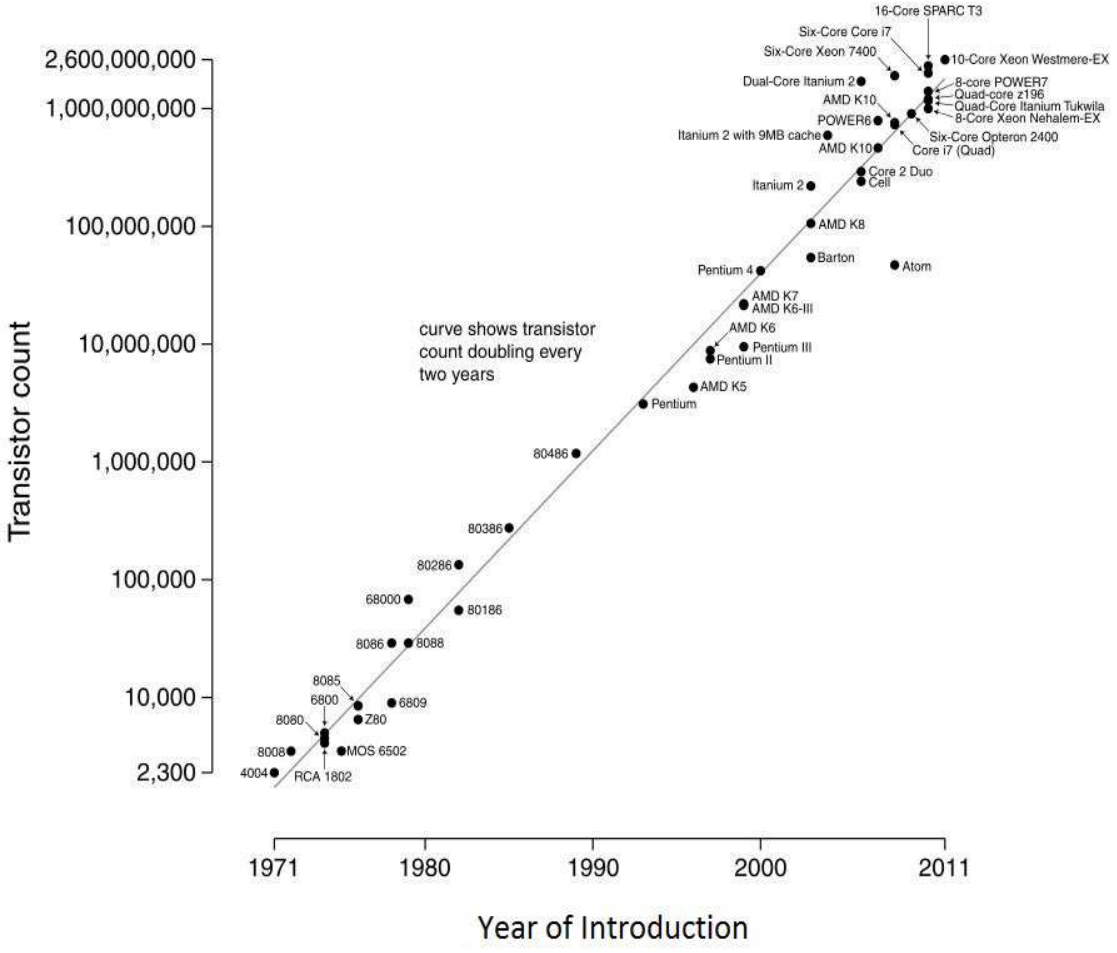

Figure 1.1: Microprocessor Transistor Counts from 1971-2011 and Moore's Law[2]

current increases, and the intrinsic capacitance decreases. Therefore, the MOSFET switching speed is improved. However, the device channel length cannot be arbitrarily reduced because of short channel effects (SCEs) such as threshold voltage roll-off and drain induced barrier lowering (DIBL) etc. There are various approaches to circumvent the scaling limits:

1. Continuously scaling down the MOSFET without changing the oxide thickness
2. Change the device structure such that the devices can be scaled further down while the SCEs are still under control.
3. Change the gate material such that the effective insulator thickness is decreased without decreasing the physical insulator thickness.

Table 1.1: Scaling rules for MOSFET devices[4]

Physical parameter	Constant Electric Field Scaling Factor	Generalized Scaling Factor	Generalized Selective Scaling Factor
Channel Length, Insulator Thickness	$1/\alpha$	$1/\alpha$	$1/\alpha_d$
Wiring Width, Channel Width	$1/\alpha$	$1/\alpha$	$1/\alpha_w$
Electric Field in Device	1	ϵ	ϵ
Voltage	$1/\alpha$	ϵ/α	ϵ/α_d
On-Current per device	$1/\alpha$	ϵ/α	ϵ/α_w
Doping	α	$\epsilon\alpha$	$\epsilon\alpha_d$
Area	$1/\alpha^2$	$1/\alpha^2$	$1/{\alpha_w}^2$
Capacitance	$1/\alpha$	$1/\alpha$	$1/\alpha_w$
Gate delay	$1/\alpha$	$1/\alpha$	$1/\alpha_d$
Power dissipation	$1/\alpha^2$	ϵ^2/α^2	$\epsilon^2/\alpha_d\alpha_w$
Power density	1	ϵ^2	$\epsilon^2\alpha_w/\alpha_d$

Research into the problems associated with the scaling as led to development of several alternatives. These include

- The use of high dielectric
- Strained silicon technology
- Multi-gate MOSFETs

Among those new device structures, one of the most important device structure is DG MOSFET, in which there are two gates on both sides of the channel. In principle, DG MOSFETs can be scaled to the shortest channel length possible for a given gate oxide thickness, because the bottom gate can effectively screen the field penetration from the drain, hence suppress the SCEs. The advantages of DG MOSFETs include: ideal 60mV/decade subthreshold slope; scaling by silicon film thickness without high doping; setting of threshold voltage by gate work functions etc. [5]. In DG MOSFET [6, 7], the top and bottom gates can be driven together to obtain larger I_{on}/I_{off} ratio, or independently to allow for dynamic threshold voltage modulation.

1.2 General terms used

Fermi level "Fermi level" [8] is the term used to describe the top of the collection of electron energy levels at absolute zero temperature. This concept comes from Fermi-Dirac

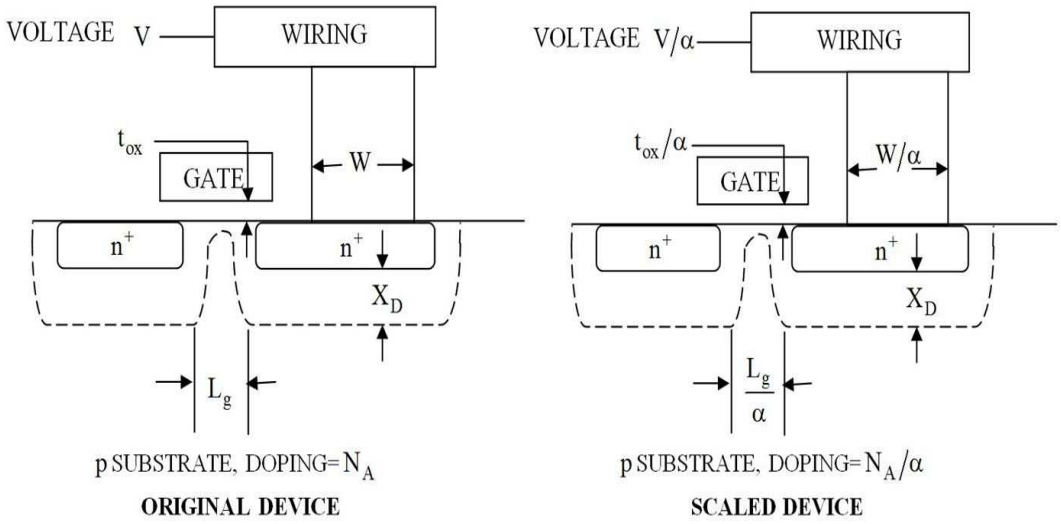

Figure 1.2: The scaling principle of silicon technology [4]

statistics. Electrons are fermions and as the Pauli Exclusion Principle cannot exist in identical energy states at absolute zero, they pack into the lowest available energy states and build up a "Fermi sea" of electron energy states. The Fermi level is the surface of that sea at absolute zero where no electrons will have enough energy to rise above the surface. The concept of the Fermi energy is a crucially important concept for the understanding of the electrical and thermal properties of solids. Both ordinary electrical and thermal processes involve energies of a small fraction of an electron volt. But, the Fermi energies of metals are of the order of electron volts. This implies that the vast majority of the electrons cannot receive energy from those processes because there are no available energy states for them to go to within a fraction of an electron volt of their present energy. Limited to a tiny depth of energy, these interactions are limited to "ripples on the Fermi Sea". At higher temperature, a certain fraction characterized by the Fermi function will exist above the Fermi level. The Fermi level plays an important role in the band theory of solids. In doped semiconductors, p-type and n-type, the Fermi level is shifted by the impurities, illustrated by their band gaps. The Fermi level is referred to as the electron chemical potential in other contexts. An important parameter in the band theory is the Fermi level, the top of the available electron energy levels at low temperatures. The position of the Fermi level with the relation to the conduction band is a crucial factor in determining electrical properties.

Energy band diagram of an MOS capacitor [8] The energy band diagram contains the

electron energy levels in the MOS structure as delineated with the Fermi energy in the metal and semiconductor as well as the conduction and valence band edge in the oxide and the silicon. The electron energy is assumed to be zero deep into the semiconductor. The oxide has band energy gap of 8 eV and the silicon has band energy gap of 1.12 eV. There are four modes of operation: Flat band, Depletion, Inversion and Accumulation. Flat band conditions exist when no charge is present in the semiconductor so that the silicon energy band is flat. Initially, we will assume that this occurs at zero gate bias. Surface depletion occurs when the holes in the substrate are pushed away by a positive gate voltage. A more positive voltage also attracts electrons (the minority carriers) to the surface which form the so-called inversion layer. Under negative gate bias, holes are attracted from the p-type substrate to the surface, yielding accumulation.

Flat band conditions [8] The flat band diagram is by far the easiest energy band diagram. The term flat band refers to fact that the energy band diagram of the semiconductor is flat, which implies that no charge exists in the semiconductor. The flat band voltage is obtained when the applied gate voltage equals to the work function difference between the gate metal and the semiconductor. However, if there is also a fixed charge in the oxide and/or at the oxide-silicon interface, the expression for the flat band voltage must be modified accordingly.

Surface depletion [8] As a more positive voltage than the flat band voltage is applied, a negative charge builds-up in the semiconductor. Initially, this charge is due to the depletion of the semiconductor starting from the oxide semiconductor interface. The depletion layer width further increases with increasing gate voltage.

Inversion layer formation [8] As the potential across the semiconductor increases beyond twice the bulk potential, another type of positive charge emerges at the oxide semiconductor interface. This charge is due to minority carriers which form a so-called inversion layer. With further increase in the gate voltage, the depletion layer width increases since the charge in the inversion layer increases exponentially with the surface potential.

Accumulation [8] Accumulation occurs when one applies a voltage less than the flat band voltage. The negative charge on the gate attracts holes from the substrate to the oxide-semiconductor interface. Only a small band bending is needed to build up the accumulation charge so that, almost all of the potential variation is within the oxide.

1.3 DG MOSFET

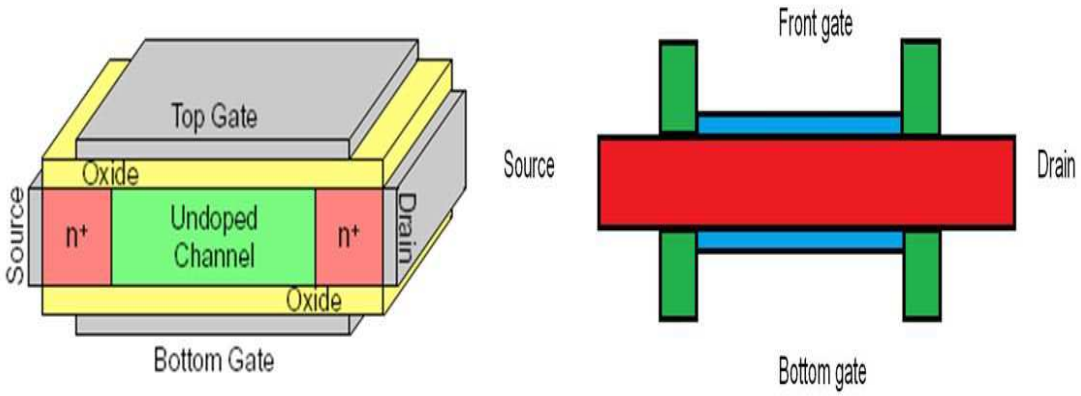

Figure 1.3: Cross-sectional view of DG MOSFET

Currently, CMOS technology is progressing to the 30nm regime. While it is widely believed that CMOS will still be the dominant technology in the near future, practical and fundamental limits of CMOS scaling poses tremendous challenges beyond 45nm technology node [9, 10]. These limits are mainly identified to be

1. Severe SCEs including threshold voltage roll-off, sub-threshold slope degradation and strong DIBL effect.

2. Quantum mechanical tunneling current including direct tunneling through the gate oxide and band to band tunneling between the substrate and drain.

3. Random dopant fluctuation effect which gives rise to threshold voltage variation from device to device.

These effects lead to unacceptably high leakage current and constitute the limiting factors of CMOS scaling at present .

To seek possible alternatives for bulk MOSFETs beyond 30nm technology node, a number of novel multi-gate MOSFETs have been proposed, including Surrounding Gate [11], Pi-Gate [12], Omega-Gate [13], Tri-Gate [14]and DG MOSFETs. Numerical simulation and analysis have shown better scalability of multi-gate MOSFETs over bulk MOSFETs. The better scalability allows multi-gate MOSFETs to scale down to shorter gate length with same off-current or produce less off-current with same gate length, thereby achieving better power-speed product. Among these new emerging devices, the DG MOSFET is most promising because of its compatibility with conventional planar technology. The DG MOSFETs are

the devices, which are having two gates on either side of the channel. Therefore the channel is surrounded by the gate material on both the sides. One on the upper side, known as top gate and the other one is in the lower side of the channel, known as bottom gate. The cross-sectional view of the DG MOSFET is shown in Fig. 1.3. The fabrication process of DG MOSFET is same as conventional MOSFET. But only difference is that in DG MOSFET, the fabrication is done both sides of the channel. In the Fig. 1.3, It has been shown that the source to drain is the silicon wafer where the source and drain portions are heavily doped and the channel portion is lightly doped or undoped. A small thickness of oxide or silicon oxide layers are fabricated on both the sides of the channel. A layer of poly-silicon of the gate material is present on both side of SiO_2 or oxide layer. The DG MOSFET is of two types

1. Symmetric-DG MOSFET: If the device is having same gate material with same work function (ϕ) and same oxide thickness (t_{ox}) of both front and back gates then the device is called Symmetric DG-MOSFET.

2. Asymmetric-DG MOSFET: If the device is having different gate material (with different work function (ϕ and $\phi^{'}$) and different oxide thickness (t_{ox} and $t^{'}_{ox}$) for both front and back gate then the device is called Asymmetric DG-MOSFET.

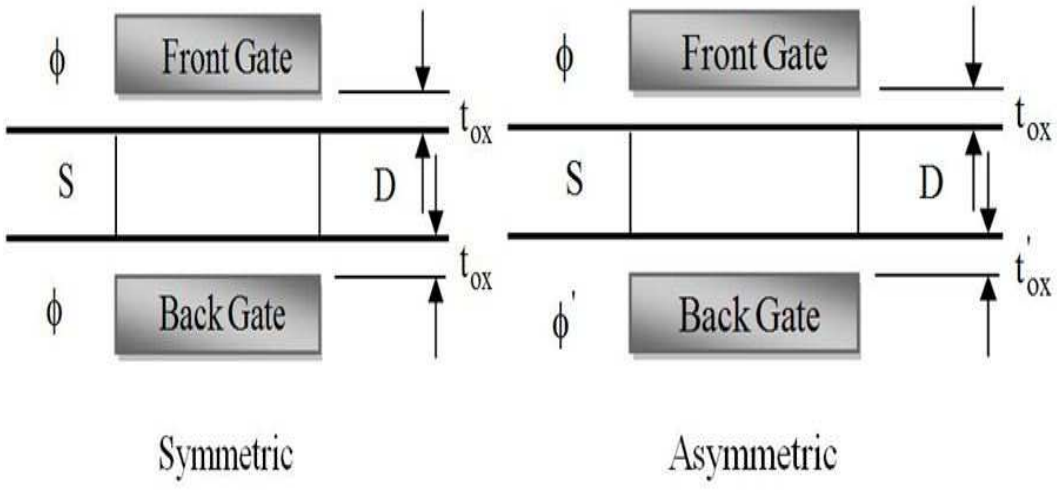

Figure 1.4: Illustration of the symmetric and asymmetric DG MOSFET

Fig. 1.4 illustrates two different types of DG MOSFETs: symmetric DG MOSFET with two gates of identical work functions and oxide thickness and asymmetric DG MOSFET

with two gates of different work functions and different oxide thickness. To fully exploit the benefits of DG MOSFETs, the body of DG MOSFETs is usually undoped or lightly doped. There are two operating modes of DG-MOSFET shown in Fig. 1.5.

1. SDDG (Simultaneously Driven Double Gate) MOSFET: In this type of operating mode of DG MOSFET, the two gates are simultaneously switched on or the bias is given simultaneously to two gates. In this case, the DG MOSFET behaves in a similar manner to a conventional MOSFET but with enhanced ON current and better control over the off state leakage-current [15].

2. IDDG (Independently Driven Double Gate) MOSFET: In this mode of operation, a bias is applied to one of the gates which dynamically changes the threshold voltage. This mode is called Independently Driven Double Gate MOSFETs. In this case, the back gate is independently biased from the front gate, thus the transfer characteristics of the DG MOSFET can vary according to the bias applied at the back gate. Thus such a device is tunable in its response to varying back gate control [15].

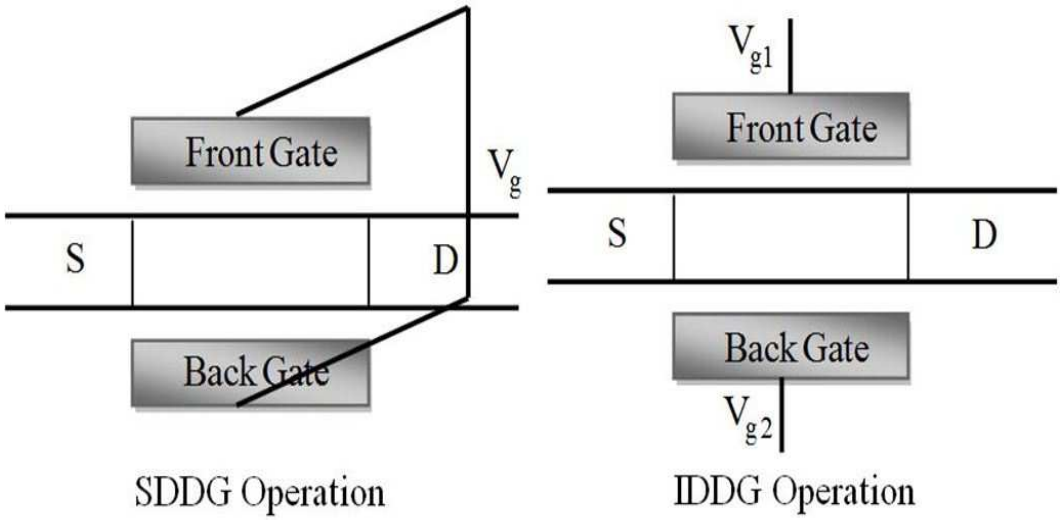

Figure 1.5: Illustration of SDDG and IDDG mode of operation

1.3.1 Advantages

The novel structure, i.e., two gates and an undoped, thin silicon film, enables DG MOSFETs to have better performance than conventional MOS transistors. The key benefits of DG MOSFETs include better SCEs, elimination of random dopant fluctuation effect and better

carrier transportation. This subsection explains the physical reasons for the advantages of DG MOSFETs over bulk MOSFETs. As VLSI technology approaches its limit, there are three primary device structures to further scale down CMOS technology: conventional bulk MOSFETs, silicon-on-insulator (SOI) MOSFETs and DG MOSFETs. The SCE is the major effect that hinders MOSFETs from further scaling down. For fully depleted SOI MOSFETs, the drain electric field can penetrate though the buried oxide into the channel region, thereby resulting in large impact on the channel electrostatics. For bulk MOSFETs and DG MOSFETs, the conducting bottom layer can screen the electric field away from the channel. Therefore, bulk MOSFETs and DG MOSFETs can achieve better SCE than fully depleted SOI MOSFETs. Simulation studies have shown that the minimum channel length imposed by SCEs for DG-MOSFET is given by

$$L_{\min} = 4.5\left(t_{si} + \frac{\varepsilon_{si}}{\varepsilon_{ox}} t_{ox}\right) \tag{1.1}$$

For bulk MOSFETs, the minimum channel length can be roughly estimated by

$$L_{\min} = 2\left(W_d + \frac{\varepsilon_{si}}{\varepsilon_{ox}} t_{ox}\right) \tag{1.2}$$

where W_d is the depletion width in bulk MOSFETs. Assuming W_d is comparable to t_{si} , evidently bulk MOSFETs can scale down further than fully depleted SOI MOSFETs solely from the SCE consideration. From (1.2), it can be seen that in order to scale down bulk MOSFETs, both W_d and t_{ox} should be reduced accordingly. Reducing W_d in bulk MOSFETs requires higher doping in the substrate. High doping in the substrate increases the junction capacitance, reduces the carrier mobility, degrades the sub-threshold slope and increases band-to-band tunneling current from the body to drain. DG MOSFETs can avoid these dilemmas by using an undoped, thin silicon body to achieve tight control of SCEs while keeping the band to band tunneling current negligible and the sub-threshold slope manageable. Simulation studies have shown that DG MOSFETs can deliver better on/off current ratio than bulk MOSFETs with the same channel length. The tight coupling between two gates leads to an ideal subthreshold slope of DG MOSFETs. When volume inversion occurs in the subthreshold region, the whole potential across the silicon film moves along with the gate voltage. This results in an ideal sub-threshold slope for long channel DG MOSFETs. The ideal sub-threshold slope allows the device to turn off fast, thus greatly reducing the leakage current while maintaining the same drive current. On the other hand, steep sub-threshold slope can also be exploited to allow the device to have lower threshold voltage and

thereby achieve larger drive current while keeping the same off current. In DG MOSFETs, the undoped body greatly reduces source and drain junction capacitances. The junction capacitance is a substantial portion of the output capacitances in bulk MOSFETs . By reducing the junction capacitance, the switching speed of DG MOSFETs can be improved. The undoped body also provides DG MOSFETs the immunity to the random dopant fluctuation effect. As CMOS further scales down, the total dopant number in the depletion region shrinks rapidly and is already in the range of fewer than 1000 dopants. Due to the discrete nature of the dopants, dopant number has a standard deviation equal to square root of the total dopants. This deviation becomes more substantial when the depletion region scales down and thereby generates an appreciable V_{th} variation from device to device. In undoped or lightly doped DG MOSFETs, the dopant fluctuation can be greatly reduced because the threshold voltage of DG MOSFET is controlled by the gate work function rather than the dopants. The elimination of depletion charges also provides an enhancement of carrier mobility for DG MOSFETs. There are two reasons for the mobility enhancement in DG MOSFETs. Firstly, the Coulomb scattering due the ionized dopants is reduced in undoped DG MOSFETs. The second enhancement comes from the reduced surface roughness scattering due to a lower surface electric field. In bulk MOSFETs, the surface electric field is given by Gausss law

$$\psi_s = \frac{Q_i + Q_d}{\varepsilon_{si}} \tag{1.3}$$

where Q_i and Q_d are the inversion and depletion charge sheet density respectively. Due to the negligible depletion charge, DG MOSFETs can be operated at a much reduced surface field for the same level of inversion charge density, which gives rise to the higher mobility.

The Device provides a better scalability option due to its excellent immunity to SCEs. Among the other advantages, it shows low drain induced barrier lowering, sub-threshold slope is near 60 mV/decade and possibility of using lightly doped and undoped body. In DG MOSFETs the inversion charges do not confine near the $Si - SiO_2$ interface but spread near the center of the channel. The charge carriers thus experiences less interface scattering, which results in increased mobility and trans-conductance in DG-Devices. The two gates of DG MOSFET placed on either side of the channel, allows effective gate control over the channel. The increased gate control enhances the drain to source currents (I_d) in ON state and prevents leakage to flow between the drain and source terminals in OFF state. It reduces the SCEs in the process and has a higher on-off current as compared to conventional MOSFET.

1.3.2 Possible Topologies

In principle, DG MOSFETs can be manufactured by either one of the three topologies in Fig. (1.5). The type I is a planar structure and it resembles the bulk MOSFET. The advantage

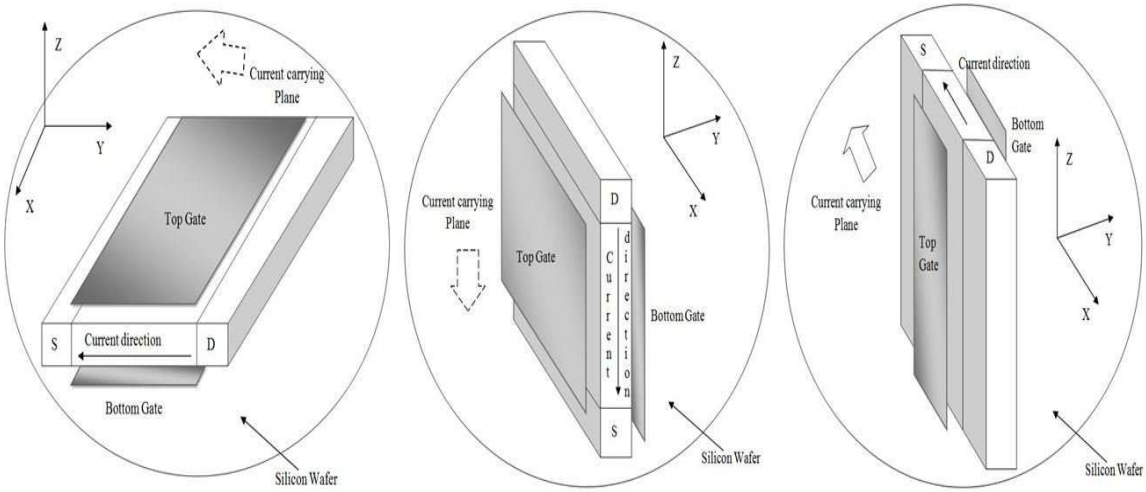

Figure 1.6: Different topologies of DG MOSFET[6]

is that the channel thickness can be controlled by thin film deposition. The limitation in fabrication of self aligned bottom gate is difficult. Therefore, misalignment may occur [6]. Type II is a vertical structure, which is hard to realize [39]. The type III is also a vertical structure. In these structures the two gates are easy to be self aligned and accessed. There are two major variations: DG FinFETs and Tri-Gate MOSFETs. If the height of the silicon film is much larger than the width. And there are effectively two gates conducting current, it forms a DG FinFET structure. If the height is comparable with the width and the top gate is also utilized to conduct current, type III structure forms a Tri-Gate MOSFET. As the top gate is activated in Tri-Gate MOSFETs, the SCE is better control by the three gates. Thus, the requirement on thin silicon thickness for the control of this effect is more relaxed in Tri-Gate MOSFETs than in FinFETs. For both FinFETs and Tri-Gate MOSFETs, a tall silicon channel is beneficial as it increases the drive current for each device. However, a tall vertical channel with precise uniformity control is difficult to fabricate. The limited height of the channel poses a limit on the total drive current that one device can provide, which raises a legitimate concern for layout efficiency especially for Tri-Gate MOSFETs. One approach to increase the drive current is to use multiple fins to effectively increase the device width. However, the available total drive current becomes discrete as it must be an integer number of the current of one fin, which creates an undesirable situation for circuit design. In FinFET

and Tri-Gate MOSFETs, the sidewall surface has different crystallographic orientation than the surface in bulk MOSFETs.

1.4 Review of analytical Modeling of DG MOSFET

The DG MOSFET is one of the most promising architectures for scaling CMOS devices down to nanometer size, since they allow a significant reduction of the SCEs, such as threshold voltage roll-off, drain-induced barrier lowering (DIBL) and subthreshold slope degradation etc. compared to planar single-gate MOSFETs. Moreover, in DG MOSFETs, the ultrathin channel material is preferred to be undoped. The absence of dopant atoms in the channel material eliminates adverse effects, such as mobility degradation and random microscopic fluctuations of dopant atoms, which can lead to unwanted dispersion in the device characteristics. Because of such advantages, an analytic current-voltage model for undoped (or lightly-doped) DG MOSFETs is highly desirable in order to facilitate the design of future nanoscale integrated circuits using these devices.

The DG MOSFET devices can be downscaled below 50 nm [2, 16, 17]. Due to the DG design, the gain of the gates increases the electrostatic control of the channel. And the SCEs can be drastically suppressed. Apart from the benefit of allowing a shorter channel, the DG MOSFETs can achieve a higher packing density due to their enhanced current drive, compared to conventional MOSFETs. The downscaling of device dimensions was the primary factor leading to improvements in integrated-circuit performance and cost, which contributes to the rapid growth of the semiconductor industry. However, small-signal parameters and SCEs, such as threshold voltage roll-off, drain-induced barrier lowering (DIBL) and subthreshold swing degradation, cannot be neglected for channel lengths below 100 nm [18]. Several works have reported that the new structures of the DG MOSFETs with high performance and scalability can be used for nanoscale analog and digital circuits [19]. In order to improve device immunity against SCEs and the small-signal parameters, new design approaches are required to enhance the reliability and electrical performance of the devices for nanoscale digital and analog applications. Numerous authors have modeled and studied the sub-threshold and saturation behavior of the nanoscale DG MOSFET [20, 21, 22, 23]. In addition, there is few studies to investigate the global electrical performance optimization (subthreshold and small-signal parameters) of the nanoscale DG MOSFETs by using a global evolutionary-based optimization technique. One preferable approach is the multi objective based optimization, which could provide practical solutions for the nanoscale CMOS circuit

design. The first step of our approach consists of an accurate compact modeling of subthreshold and small signal parameters for nanoscale DG MOSFETs. The different compact models can be used in our study as objective functions. They are given as a function of input design variables. The design of optimal nanoscale DG MOSFETs will require new insights into the underlying physics, especially quantum- mechanical (QM) treatment of the carriers confined in very thin Si films. QM confinement of inversion-layer carriers significantly affects the drain current behavior of highly scaled MOSFETs . Therefore, an accurate analytical modeling of DG MOSFETs with arbitrary Si-film thickness is needed for a physical insight and a reliable optimization approach. The nanoscale DG MOSFETs introduce challenges to compact modeling associated with the enhanced coupling between the electrodes (source, drain and gates), quantum confinement, ballistic or quasi-ballistic transport, gate tunneling current, etc. . However, in this compact model, the subthreshold parameter and the quantum confinement for a very thin silicon channel (less than 5 nm) have not been taken into account. It has been shown that in many literature, using the centroid, instead of the $Si - SiO_2$ interface for the carrier distribution, is a good choice to model the device electrostatics. In addition, Lopez-Villanueva, Baccarani and Reggiani modeled the inversion centroid charge to overcome the strong variations of the surface potential [21, 24, 25]. However, in these works, a closed form model for the drain current was not provided, thus limiting the model use by our MOGA-based design approach. In [21], an analytical model of the inversion charge including many fitting parameters by considering only channel thickness effect and ignoring the device dimensions and biases effects were suggested.

1.5 Outline of the Thesis

This work focuses on the performance analysis of symmetrical DG-MOSFET. The primary goal of the work is to study, derive and minimize the SCEs by using Multi-Objective Genetic Algorithm. This Thesis consists of five chapters.

- The first chapter contains a review of the existing literature and some preliminaries required to follow up the remaining chapters such as Moore's law, scaling, introduction to the SCEs, introduction to DG MOSFET, types of DG MOSFET, operation of DG MOSFETs and advantages of DG MOSFET.

- In the second chapter, one dimensional analytical solution is studied for an undoped (or lightly doped) DG MOSFET by incorporating only the mobile charge term in Poisson's equation [27]. The solution gives the closed form of band bending as a function of

silicon thickness and gate voltage. The analytical modeling shows the band bending across the silicon surface and becomes flat at the center. It also shows that how the electric potential varies with position. The electron volume density is also analyzed with respect to the position.

- In the third chapter, one-dimensional drain current modeling of DG MOSFET has been studied by taking only the mobile charge carriers [27, 28, 29]. It shows the $I_d - V_d$ characteristics of DG MOSFET with different values of V_g. In semiconductors when a strong enough electric field is applied, the carrier velocity in the semiconductor reach a maximum value i.e. saturation velocity. When this happens the semiconductor is said to be in a state of velocity saturation. In this chapter, the velocity saturation has also been analyzed by changing the gate voltage. Then, the two-dimensional analytical threshold modeling [32] investigates different short channel effects like Threshold voltage roll-off, Sub-threshold swing and DIBL. The SCEs are further analyzed with respect to thickness of silicon and silicon dioxide.

- In the fourth chapter, to validate the models mention in the previous chapter, the analysis has been carried out using ATLAS device simulator. It has been done by changing the length of the channel, thickness of the silicon and oxide layer [41]. It describes at what dimension, the device performs well with high on current and low SCEs. The further analysis has been done to reduce the SCEs by adopting the Graded Channel engineering technique followed by change in S/D doping concentration and has been compared with the existing result [41].

- Next, the fifth chapter is the important chapter of the thesis. In this chapter, the short channel effects are taken as objective function. The main aim of this chapter is to optimize the short channel effects by using an user friendly optimization tool box Multi Objective Genetic Algorithm (MOGA) by changing five variables or design parameters of the DG MOSFETs. (t_{ox}, t_{si}, L, V_g and V_d). To validate the model, these above designed parameters are considered to build the model by ATLAS simulator and the performance of the model is studied by comparing the results with existing results [32].

- In the Last chapter, i.e. sixth chapter concludes the thesis with some future direction of research.

CHAPTER 2

Modeling and Analysis of undoped Symmetrical DGMOSFET

This chapter considers the study of analytical modeling of undoped symmetrical DG MOSFET [27]. Same voltage is applied to the two gates having same work function. The device is considered to be undoped (lightly doped). Therefore, the absence of dopant atoms in the channel reduces mobility degradation by eliminating impurity scattering. It also avoids unwanted dispersion in the characteristics. The use of a lightly doped or undoped body is desirable for immunity against dopant fluctuation effects which give rise to threshold-voltage variation, reduced drain-to-body capacitance and higher carrier mobility which improves the circuit performance [26].

2.1 Introduction

This chapter considers a symmetric undoped (lightly doped) DG MOSFET. To study the electric potential, one-dimensional(1-D) Poisson's equation is solved, which ultimately derives the analytical expressions for band bending and inversion charge density as a function of thickness of the silicon layer and gate voltage. It also describes the relation between the threshold voltage, work function and electric potential with thickness of the silicon layer and oxide layer.

The schematic diagram of symmetric, undoped DG MOSFET is shown in the Fig. 2.1. The channel is undoped or lightly doped. The source and drain regions are heavily doped. The two gates are biased simultaneously with gate voltage V_g.

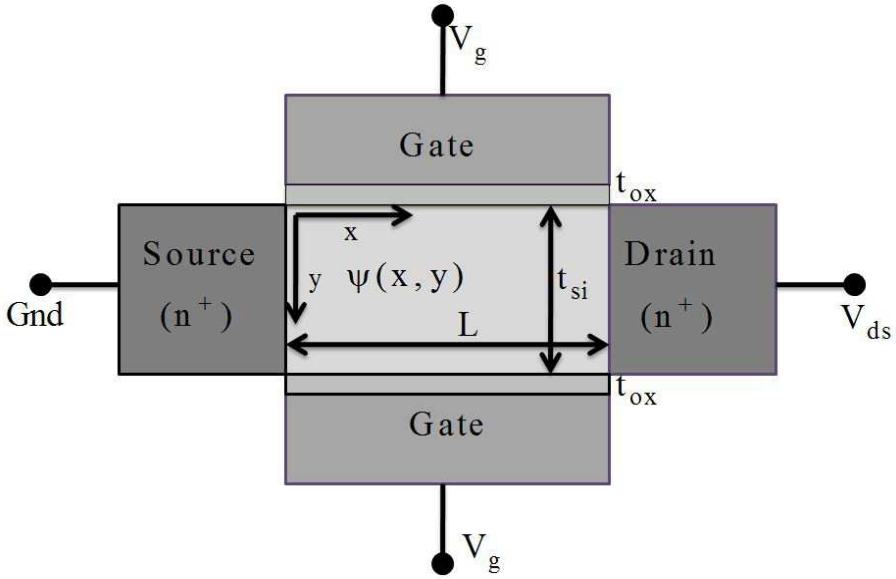

Figure 2.1: Schematic structure of undoped symmetric DG N-MOSFET

where t_{si}= Thickness of the channel,
L is the length of the channel,
X-coordinate represents the length of the channel,
Y-coordinate represents the thickness of the channel,
$\psi(x, y)$ represents the surface potential at any point on the channel surface,
t_{ox} is the thickness of the oxide layer,
V_g is the gate voltage,
V_{ds} is the drain to source voltage.

2.2 Band Diagram

The schematic band diagram of a symmetric DG MOSFET is shown in the Fig. 2.2. Same voltage is applied to the two gates having the same work function. At zero gate voltage, the position of the silicon band is largely determined by the doping concentration of the channel. This is because as long as the thin silicon is lightly doped and the depletion charge is negligible, the band remains essentially flat throughout the thickness of the film. Since, there is no contact to the silicon body, the energy levels are referenced to the electron quasi-fermi level or the conduction band of the n^+ source drain, which is represented by the long dotted line in Fig. 2.2. As the gate voltage increases towards the threshold voltage shown in Fig. 2.2, mobile charge or electron density becomes appreciable and the conduction band of the silicon body moves nearer to the conduction band of the source drain.

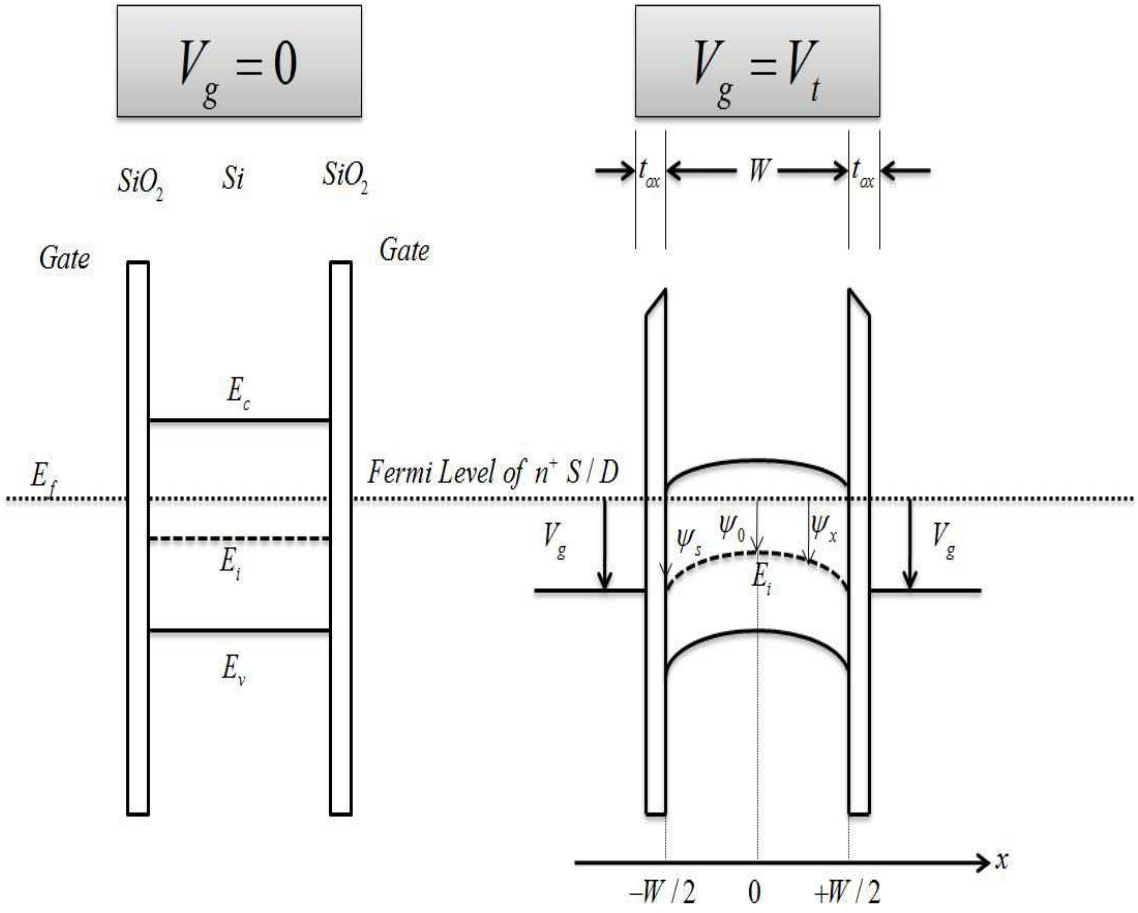

Figure 2.2: Schematic band diagrams of a symmetric, undoped DG N-MOSFET

In the Fig. 2.2, $E_f = 0$ is the Fermi Level of the n^+ Source and Drain, E_i is the intrinsic

semiconductor layer of Fermi Level of gate electrode, W is the width of the channel, t_{ox} is the thickness of the oxide layer, V_g is the gate voltage, ψ_0 is the electric potential at the center, $\psi(x)$ is the electric potential at any point and ψ_s is the electric potential at the surface.

At zero gate voltage ($V_g = 0$), the silicon bands are flat for the gate work function (slightly toward n^+ than the midgap work function) shown in the Fig. 2.2. When $V_g = V_{th}$, the conduction band of the silicon body at the surface is bent to near the conduction band of the n^+ source-drain (Long dotted line). As the gate voltage increases towards the threshold voltage in Fig. 2.2, electron charge density becomes appreciable when the conduction band of the silicon body moves near to the conduction band of the source-drain. When $V_g = 0$, or less than V_{th}, ψ_0=$\psi(x)$=ψ_s=V_g. When $V_g = V_{th}$, the band bends and ψ_0<$\psi(x)$<ψ_s<V_g.

By defining the coordinates and potential as in Fig. 2.2, we can write Poisson's equation for the silicon region with only the mobile charge (electron) density as [27]

$$\frac{d^2\psi}{dx^2} = \frac{qn_i}{\varepsilon_{si}} \mathrm{e}^{q\psi/kT}, \tag{2.1}$$

where q is the electronic charge,
ε_{si} is the permittivity of silicon,
n_i is the intrinsic carrier density,
ψ is the electric potential of the silicon surface,
K is the Boltzmann's constant,
T is the Temperature of the silicon film in Kelvin,
E_c is the conduction band of source and drain,
E_v is the valence band of source and drain.
From Fig. 2.2, at $V_g = 0$, the silicon bands are flat. At $V_g = V_{th}$, the conduction band of the silicon body at the surface is bent near the conduction band of n^+ source drain terminal.

Here, we consider an N-MOSFET with $^{q\psi}\!/_{kT} >> 1$, so that the hole density is negligible. Integrating 2.1, once with the symmetry boundary condition $^{d\psi}\!/_{dx}\,\big|_{x=0} = 0$, one can obtain

$$\frac{d\psi}{dx} = \left[\frac{2kTn_i}{\varepsilon_{si}}(\mathrm{e}^{q\psi/kT} - e^{q\psi_0/kT})\right]^{1/2}. \tag{2.2}$$

For $0 \le x \le W/2$, at $x = 0$, $\psi = \psi_0$ is the potential at the center of the silicon film to be solved later as a function of V_g. To obtain potential, integrating again, which will give us

potential as a function of x

$$\psi = -\left\{ \frac{2kT}{q}.\ln\left[\cos\left(\sqrt{\frac{q^2 n_i}{2\varepsilon_{si}kT}}.e^{q\psi_0/2kT}.\ x\right)\right]\right\} + \psi_0. \tag{2.3}$$

A study has been made for the analysis of electric potential with respect to position.

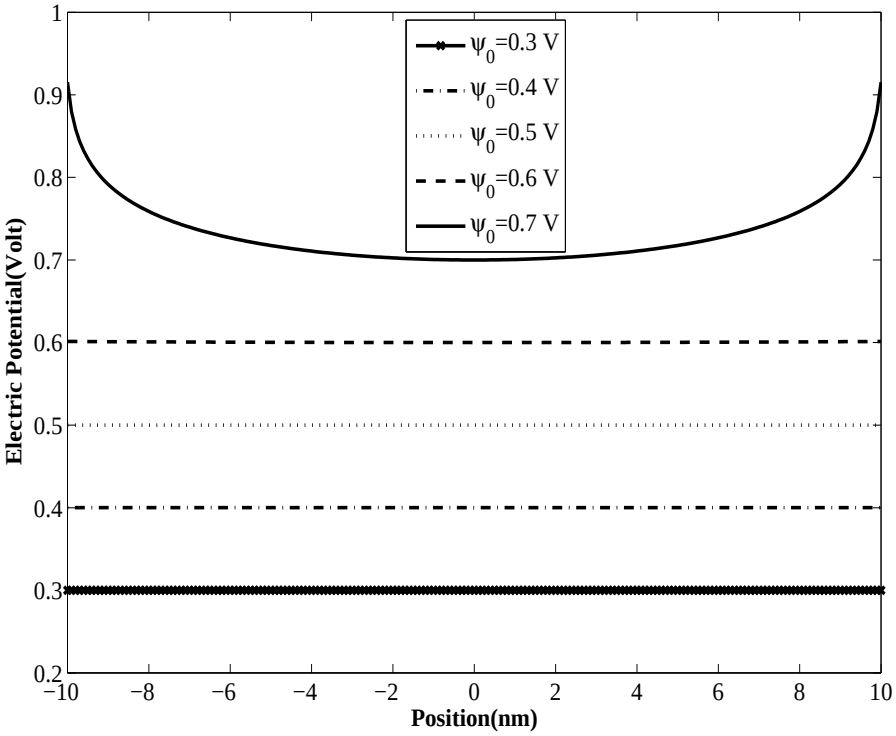

Figure 2.3: Electric Potential w.r.t Position

From the Fig. 2.3, it can be observed that the band is flat for few values of ψ_0 and the bending can also properly viewed as the electric potential increases. As the gate voltage increases, the electric potential on the silicon also increases. The electric potential at the center is equal to ψ_0 and the potential at the surface is ψ_s. As the gate voltage increases and reaches the threshold value, both ψ_0 and ψ_s increase proportionally. Therefore, up to a certain value of electric potential the band remains flat. But, as the gate voltage increases further, the ψ_0 becomes constant and ψ_s increases slowly as we move towards the surface. Therefore, at higher electric potential the device shows the band bending. At the center, the electric potential is constant and the band bends slowly from the center to the silicon surface. To check the band bending at a particular value of ψ_0, the variation of potential

with respect to position at $\psi_0 = 0.4729$ is studied in Fig. 2.4. It can be visualized from the Fig. 2.4 that there is a band bending at $\psi_0 = 0.4729$ but the bending is so small that surface potential is nearly equal to 0.4729 so it can be considered as a straight line.

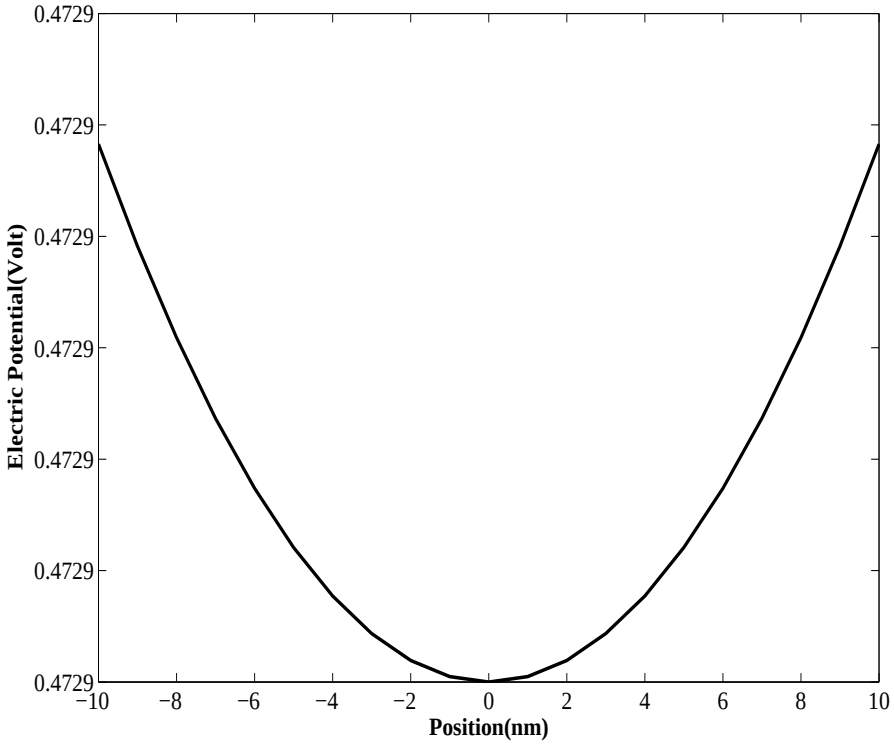

Figure 2.4: Electric Potential w.r.t Position at $\psi_0 = 0.4729$

To study the surface potential at the surface of silicon and oxide layer, the expression for potential at surface is derived from the equation (2.3).
At, x=W/2, $\psi = \psi_s$, (2.3) is given by

$$\frac{q(\psi_s - \psi_0)}{2kT} = -\ln\left[\cos\left(\sqrt{\frac{q^2 n_i}{2\varepsilon_{si}kT}}e^{q\psi_0/2kT}.(W/2)\right)\right]. \tag{2.4}$$

To study the effect of bending, the variation of surface potential with respect to mid potential is shown in the Fig. 2.5. It is clearly viewed from the Fig. 2.5, that there is a prominent bending in potential beyond ψ_0 is greater than 0.6 Volt. From the figure, it has been seen that up to certain value of electric potential, ψ_0=ψ_s, then ψ_s increases slowly. The potential at the center reaches a saturation value and it becomes constant after certain limit of electric potential but the surface potential increases exponentially as the electric potential increases.

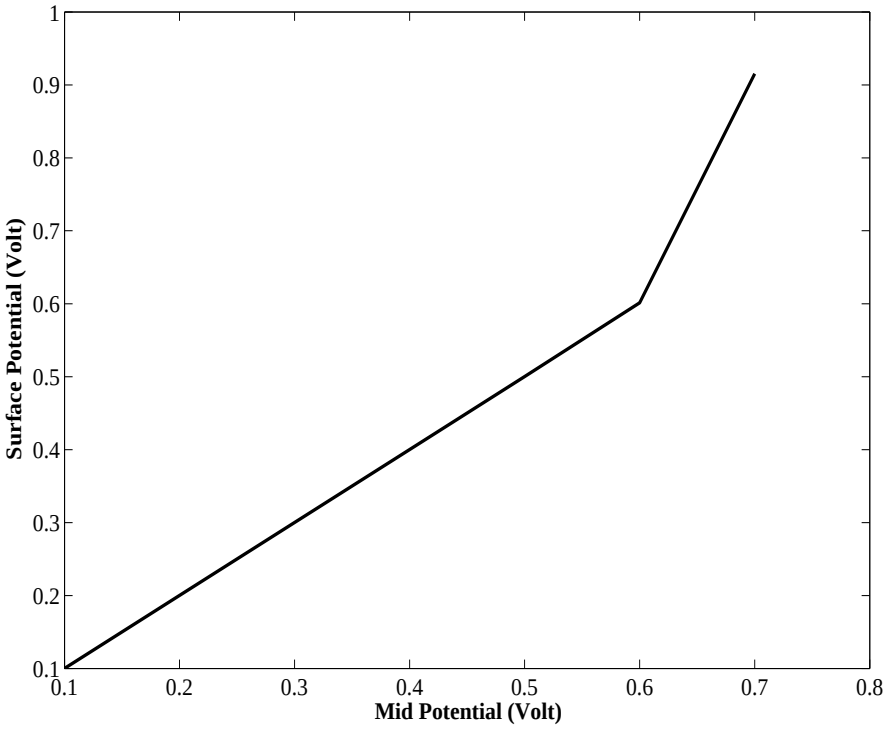

Figure 2.5: Electric Potential w.r.t Mid-potential

ψ_s is also related to V_g and t_{ox}through the boundary condition at the $Si-SiO_2$ interface:

$$\varepsilon_{ox}\frac{V_g-\Delta\phi_i-\psi_s}{t_{ox}}=\varepsilon_{si}\left.\frac{d\psi}{dx}\right|_{x=W/2}, \tag{2.5}$$

where ε_{ox} is the permittivity of the oxide layer, t_{ox} is the thickness of the oxide layer, $\Delta\phi_i$ is the work function difference between the gate electrode and intrinsic silicon, ψ_s is the surface potential, V_g is the gate potential and ε_{si} is the permittivity of the silicon layer. By putting the value of $\left.\frac{d\psi}{dx}\right|_{x=W/2}$, we have got

$$\varepsilon_{si}\left.\frac{d\psi}{dx}\right|_{x=W/2}=\varepsilon_{si}\left[\frac{2kTn_i}{\varepsilon_{si}}(\mathrm{e}^{q\psi_s/kT}-e^{q\psi_0/kT})\right]^{1/2}=\left[2\varepsilon_{si}kTn_i(\mathrm{e}^{q\psi_s/kT}-e^{q\psi_0/kT})\right]^{1/2}. \tag{2.6}$$

From (2.5) and (2.6)

$$\varepsilon_{ox}\frac{V_g-\Delta\phi_i-\psi_s}{t_{ox}}=\left[2\varepsilon_{si}kTn_i(\mathrm{e}^{q\psi_s/kT}-e^{q\psi_0/kT})\right]^{1/2}. \tag{2.7}$$

$$V_g - \Delta\phi_i = \psi_s + \frac{t_{ox}}{\varepsilon_{ox}}\left[2\varepsilon_{si}kTn_i(\mathrm{e}^{q\psi_s/kT} - e^{q\psi_0/kT})\right]^{1/2}. \tag{2.8}$$

then

$$V_g - \Delta\phi_i = \psi_s + \frac{\left[2\varepsilon_{si}kTn_i(\mathrm{e}^{q\psi_s/kT} - e^{q\psi_0/kT})\right]^{1/2}}{c_{ox}}. \tag{2.9}$$

Since the symmetric DG MOSFET is used, $\Delta\phi_i = 0$ and V_g is known. Equations (2.4) and (2.5) are solved to get the solution of ψ_s and ψ_0. The electron density of the device is given

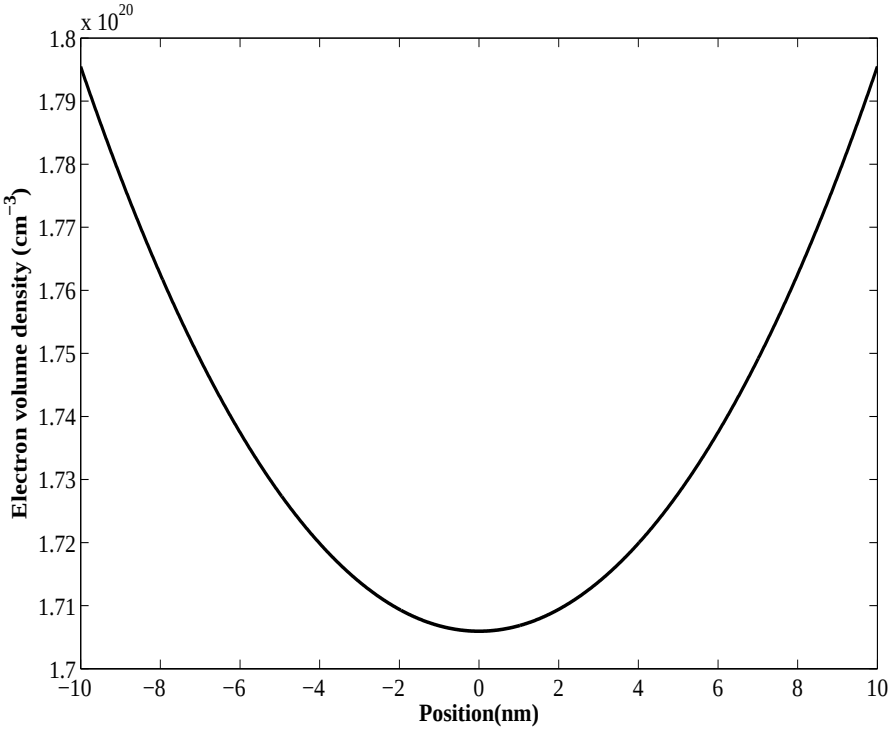

Figure 2.6: Electron Volume Density w.r.t Position

by the equation,

$$n = n_i \exp\left(\frac{q\psi}{kT}\right), \tag{2.10}$$

where n_i is the intrinsic carrier density $=8.59 \times 10^9 cm^{-3}$. The Fig. 2.6 shows that the electron density is very low at the center of the silicon. As we move towards the surface, the electron density becomes more. As the electron density increases, the concentration or the accumulation of electrons will be more towards the surface and hence the energy band of silicon bends upward.

From equation (2.3),

$$\psi = -\left\{ \frac{2kT}{q}.\ln\left[\cos\left(\sqrt{\frac{q^2 n_i}{2\varepsilon_{si}kT}}.e^{q\psi_0/2kT}.\ w/2\right)\right]\right\} + \psi_0. \tag{2.11}$$

The variation surface potential with respect to the variation center potential is shown in Fig. 2.5. As the mid potential is greater than 0.6V, the band bending is prominent. The cosine function within the bracket of the above equation (2.11) cannot exceed $\pi/2$. Because if the cosine function exceed $\pi/2$, the result will be negative value. The $ln\,(\ -\text{ve Result})$ is not valid. If the cosine function is within $\pi/2$, then result will be positive. The $ln\,(+\text{ve result}) = (\ -\text{ve})$ result. The $-$ (-ve ln result) $=$ (+ve) value, which gives increasing value of electric potential ψ with respect to ψ_0 as we move away from the center. For finding the maximum range of ψ_0

$$\left(\sqrt{\frac{q^2 n_i}{2\varepsilon_{si}kT}}.e^{q\psi_0/2kT}.\ W/2\right) = \pi/2. \tag{2.12}$$

Squaring both sides and solving the above equation, we may write ,

$$\frac{q^2 n_i}{2\varepsilon_{si}kT}.e^{q\psi_0/2kT}.\ W^2 = \pi^2. \tag{2.13}$$

we may get

$$e^{q\psi_0/2kT} = \frac{2\pi^2\varepsilon_{si}kT}{q^2W^2n_i}. \tag{2.14}$$

$$\frac{q\psi_0}{kT} = \ln\left(\frac{2\pi^2\varepsilon_{si}kT}{q^2W^2n_i}\right). \tag{2.15}$$

$$\psi_0 = \frac{kT}{q}.\ln\left(\frac{2\pi^2\varepsilon_{si}kT}{q^2W^2n_i}\right). \tag{2.16}$$

The above equation gives the saturation value of ψ_0. From (2.9), it has been seen that ψ_s increases slowly as we move away from the center of the channel in both the sides, with the term $e^{q\psi_0/kT}$ in the square root is neglected, which gives the equation below,

$$\psi_s = V_g - \Delta\phi_i - \tfrac{t_{ox}}{\varepsilon_{ox}}\left[2\varepsilon_{si}kTn_i(\mathrm{e}^{q\psi_s/kT})\right]^{1/2}. \tag{2.17}$$

here $\Delta\phi_i = 0$, for symmetric DG MOSFET. The above equation shows the relationship between the gate voltage and electric potential. The change in electric potential with respect to gate voltage is shown in Fig. 2.7. The Fig. 2.7 shows the variation of Electric potential

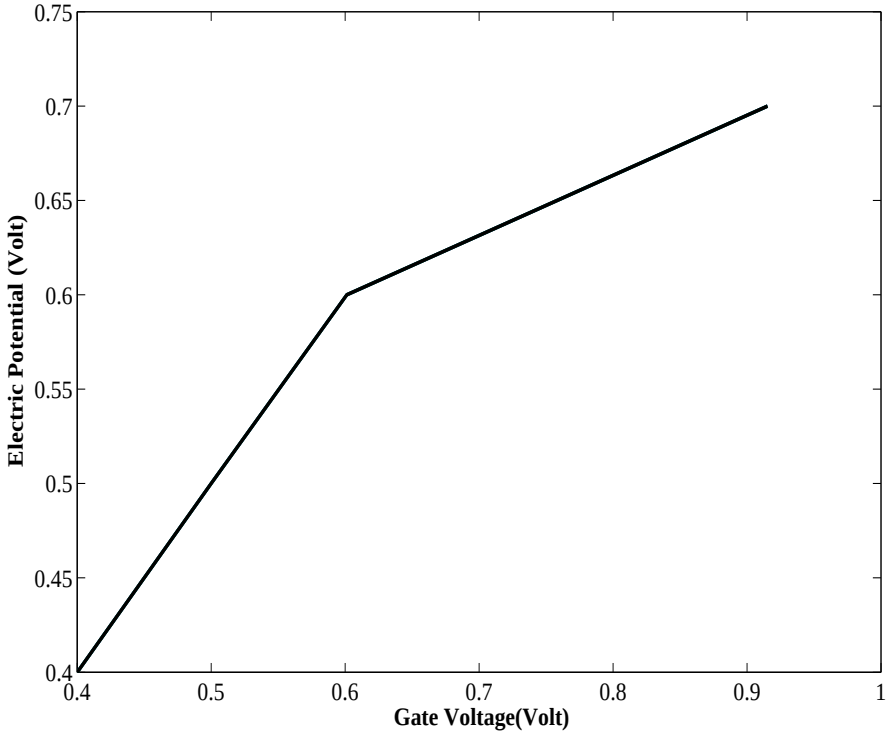

Figure 2.7: Electric potential w.r.t Gate Voltage

with respect to gate voltage at $W = 20nm$ and $t_{ox} = 2nm$. Below the threshold voltage, the mobile charge density is low and $\psi_s \approx \psi_0 \approx V_g$. In other words, the band moves as a whole as both ψ_s and ψ_0 closely follow V_g for $V_g < 0.6$. As the gate voltage increases and is greater than threshold voltage ($V_g > 0.6$), then mobile charge density near the silicon surfaces screens the gate field from the center of the silicon film and ψ_s and ψ_0 become de-coupled. The ψ_0 becomes constant and ψ_s increases exponentially.
From (2.17),

$$\psi_s = V_g - \Delta\phi_i - \tfrac{t_{ox}}{\varepsilon_{ox}}\left[2\varepsilon_{si}kTn_i(\mathrm{e}^{q\psi_s/kT})\right]^{1/2}. \tag{2.18}$$

$$\psi_s = V_g - \Delta\phi_i - [\frac{\sqrt{2\varepsilon_{si}kTn_i}}{C_{ox}}]e^{q\psi_s/2kT}. \tag{2.19}$$

Therefore,

$$\mathrm{V_g} - \ \Delta\phi_\mathrm{i} = \psi_\mathrm{s} + \left(\frac{\sqrt{(2\varepsilon_\mathrm{si}\mathrm{kTn_i})}}{C_\mathrm{ox}}\right) e^{\mathrm{q}\psi_s/2kT}. \tag{2.20}$$

The equation (2.20) shows the relationship between gate voltage, gate work function and

electric potential of the device.

2.3 Summary

- In this chapter of the thesis, an analytical study has been made for a symmetric undoped DG MOSFET by considering the mobile charge term [27]. The analysis is kept in this chapter as the background of the thesis for further work. An extensive study has been done.

- It shows the band bending starts when the gate voltage increases to the threshold voltage. Therefore, at sub-threshold region, the band becomes flat and when $V_g = V_{th}$, the band bending starts.

- The band bending also depends on the mobile charge sheet density and electron volume density.

- The gate voltage has the effect on the electric potential. In the sub-threshold region or when $V_g < V_{th}$, the band remains flat, so $\psi_0 = \psi_s = V_g$. When $V_g = V_{th}$ or $V_g > V_{th}$, $\psi_0 < \psi_s < V_g$.

CHAPTER 3

Drain Current and Threshold Voltage Modeling of DG MOSFETs

A drain current model for undoped symmetric DG MOSFET is analyzed by solving one dimensional Poisson's equation, by considering the mobile charge term and potential of quasi fermi level. An analytical expression is presented to model the behavior of the potential at the surface. It also expresses that the difference potential at the surface and the center of the undoped silicon layer as a function of silicon thickness and oxide thickness. A V-I model is derived and $I_d - V_d$ curve is plotted for different values of V_g. An expression for velocity saturation is derived from the drain current model, which proves the drain current model in strong and weak inversion.

To study the short channel effects, such as Threshold voltage roll-off, Drain Induced Barrier Lowering and Threshold Swing, an analytical threshold voltage modeling is required for the completeness of the thesis. The threshold voltage model of an undoped symmetrical DG MOSFET is based on an analytical solution of two dimensional Poisson's equation for the potential distribution. The behavior of SCEs are studied by varying different design parameters.

3.1 Analysis of Drain-Current modeling

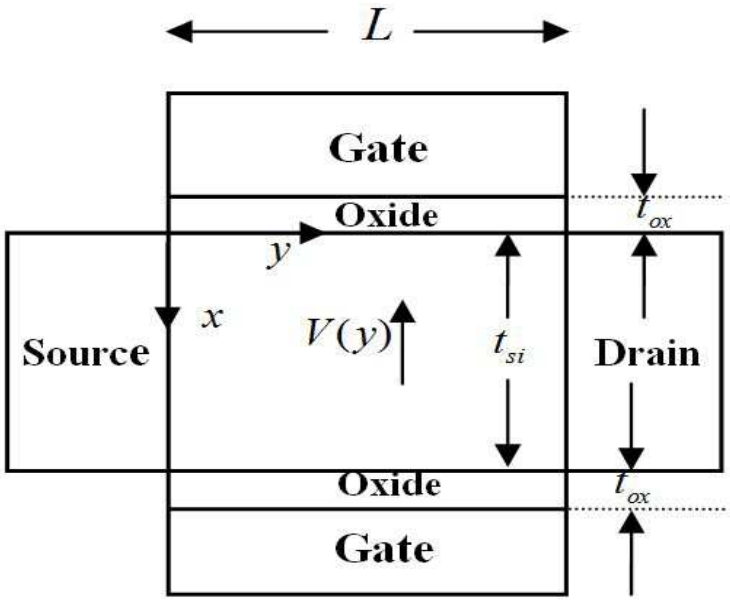

Figure 3.1: Schematic diagram of DG MOSFET with electron quasi fermi level

Consider an undoped (lightly doped) symmetrical DG MOSFET, ignoring depletion and quantum effects. The one dimensional poisson's equation in the direction vertical to the channel has been considered by neglecting hole density [28], i.e. $^{q\psi}/_{kT} >> 1$.
The one dimensional poisson's equation for the silicon is given by

$$\frac{d^2\psi(x)}{dx^2} = \frac{d^2\left(\psi(x) - V\right)}{dx^2} = \frac{qn_i}{\varepsilon_{si}} \exp\left\{\frac{q\left(\psi(x) - V\right)}{kT}\right\}, \tag{3.1}$$

where V is the electron quasi fermi potential,
Since, the current flows predominantly from the source to the drain along the y-direction, the gradient of the electron quasi-fermi potential is also in the y-direction. This justifies the gradual channel approximation that V is constant in the x-direction. Integrating (3.1),

$$\frac{d\psi(x)}{dx} = \mp\sqrt{\frac{2kTn_i}{\varepsilon_{si}} \exp\left(\frac{q\left(\psi(x) - V\right)}{kT} + C_1\right)}, \tag{3.2}$$

where C_1 is the integral constant.

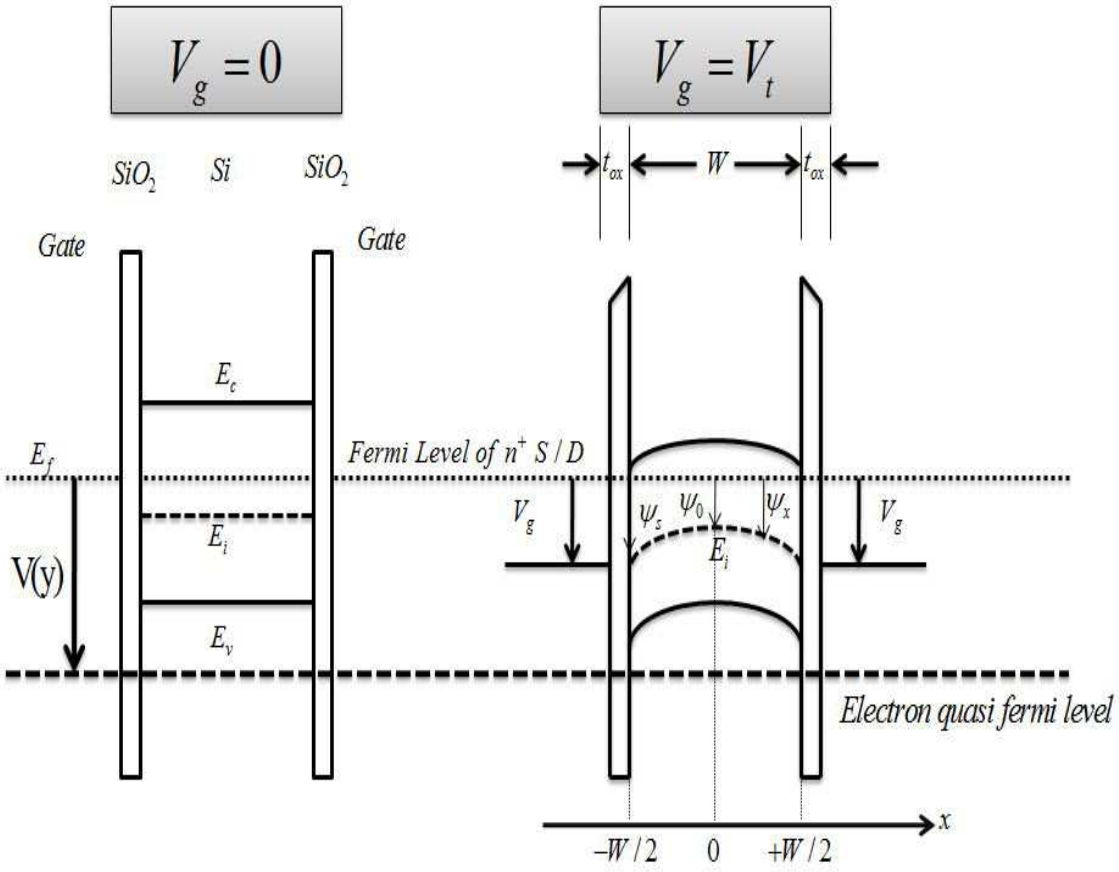

Figure 3.2: Schematic band diagrams of a symmetric, undoped Double Gate MOSFET

Integrating (3.2), once again with appropriate boundary conditions [27],

$$\psi(x) = V - \frac{2kT}{q} \ln \left[\frac{t_{si}}{2\beta} \sqrt{\frac{q^2 n_i}{2\varepsilon_{si} kT}} \cos\left(\frac{2\beta x}{t_{si}}\right) \right], \tag{3.3}$$

where β is a constant [29].

The Fig. 3.3 shows the analysis of potential variation with respect to channel length. $\psi(x)$ is also related to V_g and t_{ox} through the boundary condition at the interface as follows:

$$\varepsilon_{ox} \frac{V_g - \Delta\phi - \psi(x = \pm\frac{t_{si}}{2})}{t_{ox}} = \pm\varepsilon_{si} \frac{d\psi}{dx} \mid_{x=\pm\frac{t_{si}}{2}}, \tag{3.4}$$

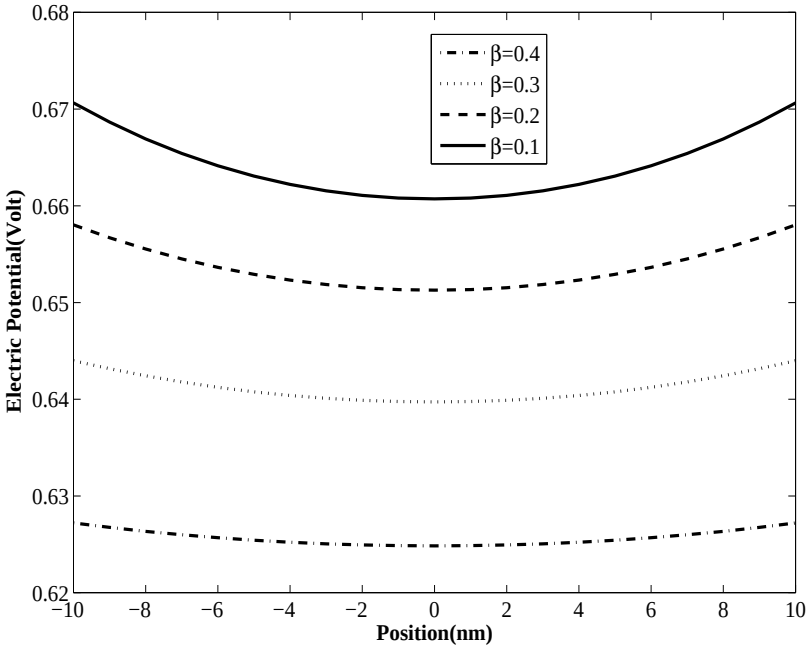

Figure 3.3: Electric Potential with respect to Position

The variation of electric potential with respect to position of the silicon channel is shown in Fig. 3.3 by setting the fermi potential at 0.01V and varying β from 0.1 to 0.6. Here, $\Delta\phi$ is the work function of both the top and bottom gate electrodes with respect to the intrinsic silicon, for symmetric gates $\Delta\phi$ is equal to zero. By putting (3.3) in (3.4), one can get [30]

$$(V_{gs} - \Delta\phi - V) + \frac{KT}{q}\log\left(\frac{qn_i t_{si}}{8C_{ox}\frac{KT}{q}}\right) - \frac{KT}{q}\log\left(\frac{C_{ox}}{C_{si}}\right) = \frac{Q}{2C_{ox}} + \frac{KT}{q}\left[\log\left(\frac{Q}{8C_{ox}\frac{KT}{q}}\right) + \log\left(\frac{C_{ox}}{C_{si}} + \frac{Q}{8C_{ox}\frac{KT}{q}}\right)\right], \tag{3.5}$$

where C_{si} is the silicon capacitance and C_{ox} is the oxide capacitance. The drain-current in a DG MOSFET is calculated as [30, 31],

$$I_{ds} = \frac{W\mu}{L}\int_0^{V_{ds}} Q(V)dV, \tag{3.6}$$

where μ is the effective mobility of the electrons, W is the width of the device and L is

the channel length.

$$dV = -\frac{dQ}{2C_{ox}} - \frac{KT}{q}\left(\frac{dQ}{Q} + \frac{dQ}{Q+2Q_0}\right), \tag{3.7}$$

where $Q_0 = \left(\frac{4KT}{q}\right) C_{si}$. Putting (3.7) in (3.6) and integrating from Q_s to Q_d, one may get

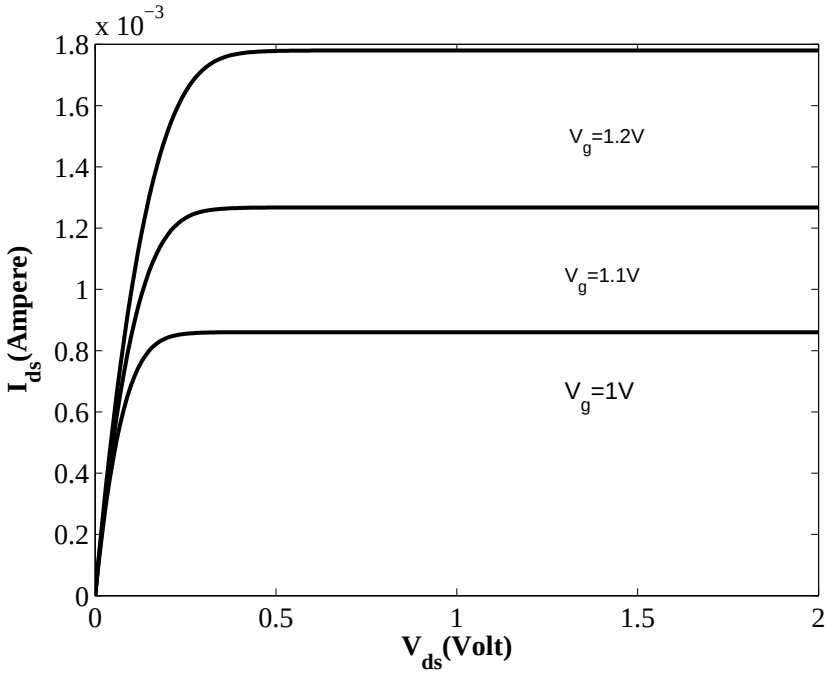

Figure 3.4: Analysis of I_d w.r.t V_d for different V_g

$$I_{ds} = \frac{W\mu}{L}\int_{Q_s}^{Q_d} Q(V)\left(-\frac{dQ}{2C_{ox}} - \frac{kT}{q}\left(\frac{dQ}{Q} + \frac{dQ}{Q+2Q_0}\right)\right), \tag{3.8}$$

where $Q = Q_s$ at the source end and $Q = Q_d$ at the drain end.
Q_s and Q_d can be computed by applying $V = 0$ and $V = V_d$ in (3.8) respectively. Integrating (3.8), one can obtain an expression of I_{ds} in terms of carrier charge density

$$I_{ds} = \frac{W\mu}{L}\left[\frac{2KT}{q}(Q_s - Q_d) + \frac{\left(Q_s^2 - Q_d^2\right)}{4C_{ox}} + 8\left(\frac{KT}{q}\right)^2 C_{si}\log\left(\frac{Q_d + 2Q_0}{Q_s + 2Q_0}\right)\right], \tag{3.9}$$

The explicit expression for Q, we use in the expression,

$$Q = 2C_{ox}\left(-\frac{2C_{ox}\beta^2}{Q_0} + \sqrt{\left(\frac{2C_{ox}\beta^2}{Q_0}\right)^2 + 4\beta^2\log^2\left[1+\exp\left(\frac{V_{gs}-V_{th}+\Delta V_{th}-V}{2\beta}\right)\right]}\right),$$

where

$Q_0 = 4\beta C_{si},$ and $\beta = \frac{KT}{q}$,

$V_{th} = V_0 + 2\beta\log\left(1+\frac{Q^{'}}{2Q_0}\right)$,

$V_0 = \Delta\phi - \beta\log\left(\frac{qn_i t_{si}}{2Q_0}\right)$

$\Delta V_{th} = \frac{\left(\frac{C_{ox}\beta^2}{Q_0}\right)Q^{'}}{Q_0+\frac{Q^{'}}{2}}$,

$Q^{'} = C_{ox}\left(-\frac{2C_{ox}\beta^2}{Q_0} + \sqrt{\left(\frac{2C_{ox}\beta^2}{Q_0}\right)^2 + 4\beta^2\log^2\left[1+\exp\left(\frac{V_{gs}-V_0-V}{2\beta}\right)\right]}\right)$.

Therefore, Q_s and Q_d in the I_{ds} expression (3.8) are analytically computed by applying $V = 0$ and $\mathrm{V} = \mathrm{V}_{ds}$ respectively,

3.1.1 Velocity Saturation

In semiconductor, when a strong enough electric field is applied, the carrier velocity in semiconductor reaches a maximum value then the semiconductor is said to be in a saturation velocity. As the applied electric field increases from the point, where velocity saturation occurs, the carrier velocity no longer increases. It is because the carrier lose energy through increased level of interaction with the lattice by emitting photons and even phonons as soon as the carrier energy is large enough to do so. If a semiconductor device enters velocity saturation, an increase in voltage applied to the device will not cause a linear increase in current as would be expected by ohm's law. Instead of the current may be increased by a small amount or not at all. The relation $V = \mu E$ is valid only at relatively low electric fields. As the electric field increases L_0 level photon emission occurs vary rapidly as the kinetic carrier energy approaches, $h\nu_{L_0}$, so that the velocity saturates. In silicon, the velocity versus field characteristic saturates at the high electric fields. At low electric fields, the electron mobility in si can be as high as $\mu = 1500cm^2/Vs$. However at high electric fields, the velocity saturates due to L_0 photon emission. The low electric field velocity versus field current can be expressed as $V(E) = \mu E$ or $V = \mu E$ but for very short gate lengths this relation does not hold because the electric field is so high that velocity saturation occurs. For high electric field, the relation is [31, 24]

$$V_{sat} = (V_{gs} - V_{th})\,\frac{\nu_{sat}}{\frac{\mu_{eff}}{2L}(V_{gs} - V_{th}) + \nu_{sat}}, \tag{3.10}$$

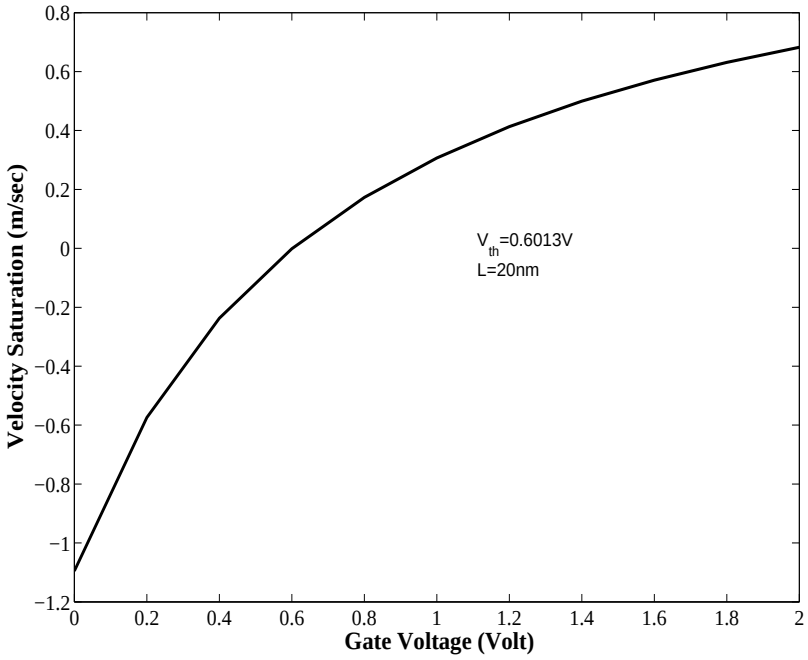

Figure 3.5: Velocity saturation w.r.t V_g

where μ_{eff} is the effective mobility, ν_{sat} is the saturation velocity and V_{th} is the threshold voltage. The validation of this equation can be proved in weak inversion by replacing $(V_{gs} - V_{th})$ by $\frac{-Q_s}{2C_{ox}}$ [31] . This term tends to $(V_{gs} - V_{th})$ in strong inversion and tends to zero in very low inversion. Q_s is the charge at the source end of the channel. In weak inversion, V_{sat} tends to zero but the theoretical value of $V_{sat} = \frac{2KT}{q}$[31]. To correct it, Q_s is replaced by Q_{seff}.
(3.10) can be

$$V_{sat} = \left(-\frac{Q_{seff}}{2C_{ox}}\right) \frac{\nu_{sat}}{-Q_{seff}\frac{\mu_{eff}}{4LC_{ox}} + \nu_{sat}}, \tag{3.11}$$

$$\frac{2KT}{q} = \left(-\frac{Q_{seff}}{2C_{ox}}\right) \frac{\nu_{sat}}{-Q_{seff}\frac{\mu_{eff}}{4LC_{ox}} + \nu_{sat}}. \tag{3.12}$$

Solving (3.12), one may get

$$Q_{seff}\left(\frac{KT}{q}\frac{\mu_{eff}}{L} - \nu_{sat}\right) = \frac{4KT}{q}\nu_{sat}C_{ox}. \tag{3.13}$$

The electron mobility μ is expressed as ,

$$\mu = \frac{\mu_{eff}}{\left(1 + \frac{\mu_{eff} V_{sat}}{\nu_{sat}(L - \Delta L)}\right)},$$

where L is the total conducting channel length, ΔL is the Length of saturation region. During velocity saturation, The current I_d is expressed as

$$I_{dseff} = \frac{W \mu_{eff}}{L_e} \left[2\frac{kT}{q} (Q_s - Q_d) + \frac{Q_s^2 + Q_d^2}{4C_{ox}} + 8\left(\frac{kT}{q}\right)^2 C_{si} \log \left[\frac{Q_d + 2Q_0}{Q_s + 2Q_0}\right]\right], \qquad (3.14)$$

where L_e is the effective gate length due to the effect of velocity saturation and is expressed as [44]

$$L_{eff} = (L - \Delta L)\left[1 + \left(\frac{\mu_{eff} V_{sat}}{v_{sat}(L - \Delta L)}\right)\right].$$

The model to be continuous during the transition to saturation regime, the effective drain voltage is equal to [40]

$$V_{dseff} = V_{sat} - V_{sat} \frac{\ln\left[1 + \exp\left(1 - \frac{V_{ds}}{V_{sat}}\right)\right]}{\ln\left[1 + \exp\left(A\right)\right]},$$

where V_d is drain voltage in linear region and A is the fitting parameter, whose value varies from 4 to 6.

3.2 Analysis of Threshold voltage Modeling

The DG MOSFET allows a significant reduction of the SCEs, such as threshold voltage roll-off, drain-induced barrier lowering (DIBL) and subthreshold slope degradation [16, 18], compared to planar single-gate MOSFETs. Moreover, in DG MOSFETs, the ultrathin channel material is preferred to be undoped. The absence of dopant atoms in the channel material eliminates adverse effects, such as mobility degradation and random microscopic fluctuations of dopant atoms, which can lead to unwanted dispersion in the device characteristics. Because

of these advantages, a simple analytic threshold-voltage model for undoped DG MOSFETs are desirable in order to facilitate the design of these devices. The SCEs in undoped DG MOSFETs are derived by a simple analytical expression for the 2-D potential distribution along the channel of symmetrical DG MOSFETs in weak inversion. Based on this analytical potential distribution, a simple analytical expression for the threshold voltage is derived for undoped DG MOSFETs. Different SCEs are to be studied to fulfill the requirement of the thesis.

A schematic cross section of a symmetric n-channel DG MOSFET and the definition of the geometrical characteristics are shown in Fig. 3.1. For operation in the weak inversion region, according to the Poisson's equation, without taking the quasi fermi voltage, the potential distribution in the silicon channel $\psi(x, y)$ is given by [32],

$$\frac{d^2\psi(x,y)}{dx^2} + \frac{d^2\psi(x,y)}{dy^2} = \frac{qN_A}{\varepsilon_{si}}, \tag{3.15}$$

with $0 \leq x \leq t_{si}$, $0 \leq y \leq L$.

where N_A is the channel doping concentration. For low values of drain voltage V_d, the potential $\psi(x, y)$ can be represented as a second-order parabolic function along the vertical x-direction:

$$\psi(x, y) = c_0(y) + c_1(y)x + c_2(y)x^2, \tag{3.16}$$

where the coefficients c_0 , c_1, and c_2 depend on y only. Defining the potential at the front interface as $\psi(0, y)$ and at the back interface as $\psi(t_{si}, y)$, due to the symmetrical structure, it holds

$$\psi_s(y) \equiv \psi_s(0, y) \equiv \psi_s(t_{si}, y), \tag{3.17}$$

By assuming vertical electric fields in the gate oxides, using Gauss's law in the x-direction, the boundary conditions in the channel-oxide interfaces can be written as

$$\left.\frac{d\psi(x,y)}{dx}\right|_{x=0} = \frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{\psi_s(y) - V_g^{'}}{t_{ox}}, \tag{3.18}$$

$$\left.\frac{d\psi(x,y)}{dx}\right|_{x=t_{si}} = \frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{V_g^{'} - \psi_s(y)}{t_{ox}}, \tag{3.19}$$

$V_g^{'} = V_g - V_{FB}$, where V_g is the Gate voltage, V_{FB} is the flat band voltage, t_{ox} is the thickness of the oxide layer, ε_{ox} is the dielectric constant of oxide, midgap metal voltage is $V_{FB} = -KT \ln\left(\frac{N_A}{n_i}\right)$, KT is the thermal energy.

Solving (3.16) to (3.19), we obtained the coefficient as

$$c_0 = \psi_s(y),$$

$$c_1 = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{\psi_s(y) - V_g^{'}}{t_{ox}},$$

$$c_2 = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{V_g^{'} - \psi_s(y)}{t_{ox} t_{si}},$$

By substituting the values of c_0, c_1 and c_2 in (3.15), it can be re-written as

$$\frac{d^2\psi_s(y)}{dy^2} - \alpha\psi_s(y) = \beta, \tag{3.20}$$

where $\alpha = \frac{2\varepsilon_{ox}}{\varepsilon_{si}t_{ox}t_{si}+\varepsilon_{ox}t_{si}x-\varepsilon_{ox}t_{si}x^2}$, $\beta = \frac{qN_At_{ox}t_{si}+2\varepsilon_{ox}V_g^{'}}{\varepsilon_{si}t_{ox}t_{si}+\varepsilon_{ox}t_{si}x-\varepsilon_{ox}t_{si}x^2}$.
Solving (3.20) with the boundary conditions $\psi_s(y) = V_{bi}$ at $x = 0$ and $\psi_s(y) = V_{bi} + V_d$ at $x = L$, where V_{bi} is the built in potential across the source/drain channel junction for which $V_{bi} = KT\ln\left(\frac{N_AN_D}{n_i^2}\right)$, where N_D is the donor concentration and n_i is the intrinsic carrier concentration. The potential distribution along the channel at the front and back gate interfaces is

$$\begin{aligned}\psi_s(y) = \frac{1}{\exp\left(\frac{2L}{\lambda_1}\right) - 1} \Bigg[&(V_{bi} + V_d - A_1)\left(\exp\left(\frac{L+y}{\lambda_1}\right) - \exp\left(\frac{L-y}{\lambda_1}\right)\right) \\ &+ (V_{bi} - A_1)\left(\exp\left(\frac{2L-y}{\lambda_1}\right) - \exp\left(\frac{y}{\lambda_1}\right)\right) + A_1\left(\exp\left(\frac{2L}{\lambda_1}\right) - 1\right)\Bigg],\end{aligned} \tag{3.21}$$

where $A_1 = V_g^{'} - \frac{qN_At_{si}t_{ox}}{2\varepsilon_{ox}}$ and $\lambda_1 = \sqrt{\frac{\varepsilon_{si}t_{si}t_{ox}}{2\varepsilon_{ox}}}$.
The parameter λ_1 is the so called natural channel length [33], which characterizes the SCEs in DG MOSFETs, assuming that the current flows along the channel. In short-channel devices, the center of the channel has higher electrostatic potential than anywhere because of the influence of the source/drain potential and the weak gate control below threshold. Thus, the natural channel length in short-channel DG MOSFETs can be described more accurately as a function of the channel depth. To get the solution satisfying the boundary conditions $\psi_s(y) = V_{bi}$ at $x = 0$ and $\psi_s(y) = V_{bi} + V_d$ at $x = L$ within the body of the silicon channel at different depths x from the front gate interface, we obtain the relation $\psi_s(y)$

and the potential $\psi_x(y)$ at a depth x corresponding to a fraction n of the silicon thickness t_{si}. By substituting $x = t_{si}/n$ (with $n \neq 0$) in (3.16) where c_i coefficients are given by (3.16)-(3.21), the relation between $\psi_s(y)$ and $\psi_x(y)$ is

$$\psi_s(y) = K\psi_x(y) + \Lambda V_g^{'}, \tag{3.22}$$

where $K = \frac{1}{1+\frac{\varepsilon_{ox}t_{si}(n-1)}{\varepsilon_{si}t_{ox}n^2}}$ and $\Lambda = \frac{1}{1+\frac{\varepsilon_{si}t_{ox}n^2}{\varepsilon_{ox}t_{si}(n-1)}}$.
It is $n \neq 0, 1$ since for n =0 or 1 (i.e., at $x = 0$ or t_{si}), the potential corresponds to the back channel interface potential given by (3.22). By substituting (3.22) in (3.15), we obtain the following differential equation:

$$\frac{d^2\psi_x(y)}{dy^2} - \alpha^{'}\psi_x(y) = \beta^{'}, \tag{3.23}$$

where $\alpha^{'} = \frac{2\varepsilon_{ox}}{\varepsilon_{si}t_{ox}t_{si}+\frac{\varepsilon_{ox}t_{si}^2}{n}-\frac{\varepsilon_{ox}t_{si}^2}{n^2}}$, $\beta^{'} = \frac{2\varepsilon_{ox}(1-\Lambda)V_g^{'}-qN_At_{ox}t_{si}}{K\left(\varepsilon_{si}t_{ox}t_{si}+\frac{\varepsilon_{ox}t_{si}^2}{n}-\frac{\varepsilon_{ox}t_{si}^2}{n^2}\right)}$.
Solving the equation (3.23) with the boundary conditions $\psi_x(y) = V_{bi}$ at $x = 0$ and $\psi_x(y) = V_{bi} + V_d$ at $x = L$

$$\begin{aligned}\psi_x(y) = \frac{1}{\exp\left(\frac{2L}{\lambda_2}\right)-1}\Bigg[&(V_{bi}+V_d-A_2)\left(\exp\left(\frac{L+y}{\lambda_2}\right)-\exp\left(\frac{L-y}{\lambda_2}\right)\right)\\&+(V_{bi}-A_2)\left(\exp\left(\frac{2L-y}{\lambda_2}\right)-\exp\left(\frac{y}{\lambda_2}\right)\right)+A_2\left(\exp\left(\frac{2L}{\lambda_2}\right)-1\right)\Bigg],\end{aligned} \tag{3.24}$$

where $A_2 = \frac{2\varepsilon_{ox}(1-\Lambda)V_g^{'}-qN_At_{ox}t_{si}}{2\varepsilon_{ox}K}$, $\lambda_2 = \sqrt{\frac{\varepsilon_{si}t_{ox}t_{si}+\frac{\varepsilon_{ox}t_{si}^2}{n}-\frac{\varepsilon_{ox}t_{si}^2}{n^2}}{2\varepsilon_{ox}}}$.
From (3.24), Two-dimensional distribution of ψ(x, y) along the channel can be represented as

$$\begin{aligned}\psi(x,y) = \frac{1}{\exp\left(\frac{2L}{\lambda_3}\right)-1}\Bigg[&(V_{bi}+V_d-A_3)\left(\exp\left(\frac{L+y}{\lambda_3}\right)-\exp\left(\frac{L-y}{\lambda_3}\right)\right)\\&+(V_{bi}-A_3)\left(\exp\left(\frac{2L-y}{\lambda_3}\right)-\exp\left(\frac{y}{\lambda_3}\right)\right)+A_3\left(\exp\left(\frac{2L}{\lambda_3}\right)-1\right)\Bigg],\end{aligned} \tag{3.25}$$

where $A_3 = V_g^{'} - qN_A\frac{\varepsilon_{si}t_{ox}t_{si}+\varepsilon_{ox}(t_{si}-x)x}{2\varepsilon_{ox}\varepsilon_{si}}$,$\lambda_3 = \sqrt{\frac{\varepsilon_{si}t_{ox}t_{si}}{2\varepsilon_{ox}}\left(1+\frac{\varepsilon_{ox}x}{\varepsilon_{si}t_{ox}}+\frac{\varepsilon_{ox}x^2}{\varepsilon_{si}t_{ox}t_{si}}\right)}$.
Let N_A is equal to zero (negligible doping or less doping), the 2-D potential distribution $\psi(x, y)$ along the channel can be expressed with good accuracy as follows

$$\psi(x,y) = V_g^{'} + \frac{1}{\exp\left(\frac{2L}{\lambda}\right) - 1}\left[\left(V_{bi} + V_d - V_g^{'}\right)\left(\exp\left(\frac{L+y}{\lambda}\right) - \exp\left(\frac{L-y}{\lambda}\right)\right)\right. \\ \left. + \left(V_{bi} - V_g^{'}\right)\left(\exp\left(\frac{2L+y}{\lambda}\right) - \exp\left(\frac{y}{\lambda}\right)\right)\right], \tag{3.26}$$

where λ is given by $\lambda(x) = \sqrt{\frac{\varepsilon_{si} t_{ox} t_{si}}{2\varepsilon_{ox}}\left(1 + \frac{\varepsilon_{ox} x}{\varepsilon_{si} t_{ox}} - \frac{\varepsilon_{ox} x^2}{\varepsilon_{si} t_{ox} t_{si}}\right)}$.

In (4.1), $V_g^{'} = V_g - \phi_{ms}$, where ϕ_{ms} is the gate work function referenced to intrinsic silicon, and V_{bi} is the built-in potential across the source/drain-channel junctions $V_{\text{bi}} = KT\ln\left(\frac{N_D}{n_i}\right)$, where N_D is the donor concentration of the source/drain contacts and n_i is the intrinsic carrier concentration.

The Fig. 3.6 shows the relation between the electric potential with the channel length and

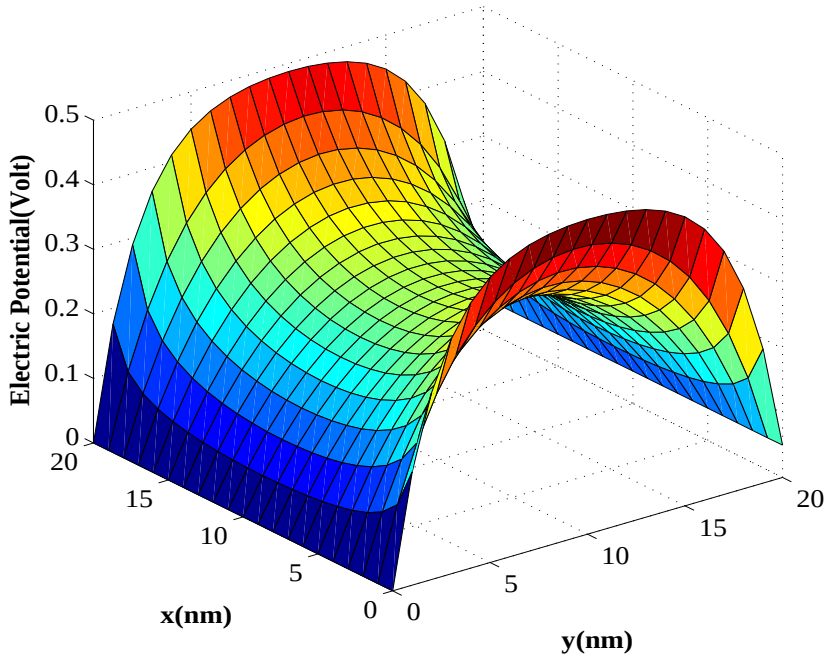

Figure 3.6: Electric Potential w.r.t Position

thickness of the channel at t_{ox}=2nm, t_{si}=20nm, L=20nm. Here, it has been seen that the potential at the center ($t_{si}/2$) is constant and the band is almost flat. As we move towards the surface the band starts bending and more bending is shown at the two surface of the silicon channel ($x = 0, x = 20$). This has been shown in a 3-dimensional view. The graph has been done by varying $x = 0$ to 20nm and $y = 0$ to 20 nm. The simple potential distribution

can be used to model the threshold voltage in DG MOSFETs. The threshold voltage V_{th} can be defined quantitatively as the gate voltage at which the minimum carrier charge sheet density Q_{inv} reaches a value Q_{th} adequate to achieve the turn on condition. The value of V_{th} at which $Q_{\text{inv}} = Q_{th}$ leads to the simple and explicit expression for the threshold voltage V_{th} [34],

$$V_{th} = \phi_{ms} + AV_{thermal} \ln\left(\frac{Q_{th}}{n_i t_{si}}\right) - B[Z]^{1/2}[Z + V_d]^{1/2} - C\left(2V_{bi} + V_d\right), \tag{3.27}$$

where $Z = V_{bi} - V_{thermal} \ln\left(\frac{Q_{th}}{n_i t_{si}}\right)$, $A = \frac{\exp\left(\frac{4L}{\lambda}\right) - 2\exp\left(\frac{2L}{\lambda}\right) + 1}{\left(\exp\left(\frac{L}{\lambda}\right) - 1\right)^4}$
$B = \frac{2\exp\left(\frac{L}{2\lambda}\right)\left(1 + \exp\left(\frac{L}{\lambda}\right)\right)}{\left(\exp\left(\frac{L}{\lambda}\right) - 1\right)^2}$, $C = \frac{2\exp\left(\frac{3L}{\lambda}\right) - 4\exp\left(\frac{2L}{\lambda}\right) + 2\exp\left(\frac{L}{\lambda}\right)}{\left(\exp\left(\frac{L}{\lambda}\right) - 1\right)^4}$,
$\lambda\left(\frac{t_{si}}{4}\right) = \sqrt{\frac{\varepsilon_{si} t_{ox} t_{si}}{2\varepsilon_{ox}}\left(1 + \frac{\varepsilon_{ox} t_{si}}{4\varepsilon_{si} t_{ox}} - \frac{\varepsilon_{ox} t_{si}^2}{16\varepsilon_{si} t_{ox} t_{si}}\right)}$, $Q_{th} = 3.2 \times 10^{10} cm^{-2}$.
For long enough channel, it is $A = 1$, and the parameters B and C tend to zero; thus, the threshold voltage expression (V_{th_long}) reduces to

$$V_{th\_long} = \phi_{ms} + V_{thermal} \ln\left(\frac{Q_{th}}{n_i t_{si}}\right). \tag{3.28}$$

The Channel length reduction induces short channel effects such as Threshold voltage roll-off, Drain Induced Barrier lowering(DIBL) and Sub-threshold Swing(SS).

3.2.1 Short Channel Effects

When the channel length is of same order of magnitude as the depletion layer widths of Source and Drain junction, the short channel effect arises. The short channel effects are the collection of several different problems that arise in a highly scaled MOSFET having a small channel length. As the channel length (L) decreases, there is an increase in both operation speed and number of components per chip. But there is a modification in threshold voltage and electron drift characteristics.

3.2.1.1 Threshold Voltage Roll-off

There are two effects in a semiconductor device threshold voltage roll-up and threshold voltage roll-off. The threshold voltage roll-up is an effect where the threshold voltage increases with respect to decrease in channel length. But, the threshold voltage roll-off is an effect where there is an decrease in threshold voltage with decrease in channel length. The voltage roll-off is an short channel effect. The threshold voltage is a voltage at which the device

turns on. With decrease in channel length, threshold voltage decreases. Therefore, at shorter channel length, the device turns on suddenly, which degrades the device performance. The parameter ΔV_{th} is defined as the threshold voltage measured at a given V_d at any gate length minus the threshold voltage of long channel. The voltage roll-off [34] is denoted as $\Delta V_{th} = V_{th} - V_{th\_long}$,

$$\Delta V_{th} = (A-1)\, V_{thermal} \ln\left(\frac{Q_{th}}{n_i t_{si}}\right) - B[Z]^{1/2}[Z+V_d]^{1/2} - C\,(2V_{bi}+V_d)\,, \tag{3.29}$$

where $Z = V_{bi} - V_{thermal} \ln\left(\frac{Q_{th}}{n_i t_{si}}\right)$, $B = \frac{2\exp\left(\frac{L}{2\lambda}\right)\left(1+\exp\left(\frac{L}{\lambda}\right)\right)}{\left(\exp\left(\frac{L}{\lambda}\right)-1\right)^2}$,
$C = \frac{2\exp\left(\frac{3L}{\lambda}\right)-4\exp\left(\frac{2L}{\lambda}\right)+2\exp\left(\frac{L}{\lambda}\right)}{\left(\exp\left(\frac{L}{\lambda}\right)-1\right)^4}$, $\lambda\left(\frac{t_{si}}{4}\right) = \sqrt{\frac{\varepsilon_{si} t_{ox} t_{si}}{2\varepsilon_{ox}}\left(1+\frac{\varepsilon_{ox} t_{si}}{4\varepsilon_{si} t_{ox}} - \frac{\varepsilon_{ox} t_{si}^2}{16\varepsilon_{si} t_{ox} t_{si}}\right)}$.

The variation of threshold voltage roll-off is shown in the Fig. 3.7 with respect to channel length for $t_{ox} = 2nm$ and $t_{si} = 5nm$. From the Fig. 3.7, it is observed that as the channel length decreases, the threshold voltage roll-off decreases [32]. The purpose is to optimize the threshold voltage roll-off with two design parameters, t_{ox} and t_{si}. So, the study of variation of threshold voltage roll-off with respect to the channel length has been studied for different values of t_{ox} and t_{si}.

In the Fig. 3.8, the analysis of threshold voltage roll-off has been shown with respect to length of the channel for three different value of t_{ox}=1nm, 2nm and 4nm , at $t_{si} = 5nm$. In fig. 3.9, the analysis has been done for three values of $t_{si} = 5nm$, 7nm and 10nm and $t_{ox} = 2nm$. From the analysis of the figures, it has been seen that the threshold voltage roll-off is more severe as the thickness of the silicon body (t_{si}) and oxide layer (t_{ox}) increases due to short channel effects.

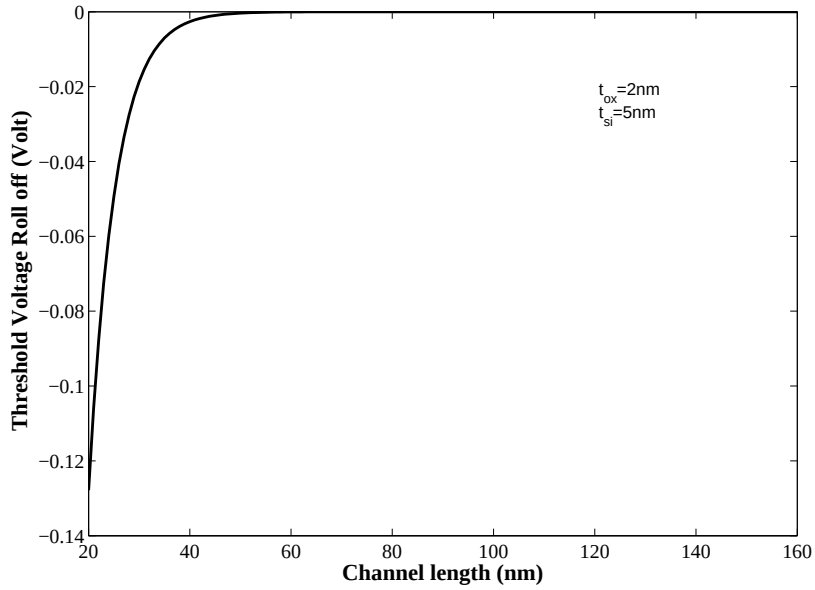

Figure 3.7: Threshold Voltage Roll-off of DGMOSFET w.r.t Channel length

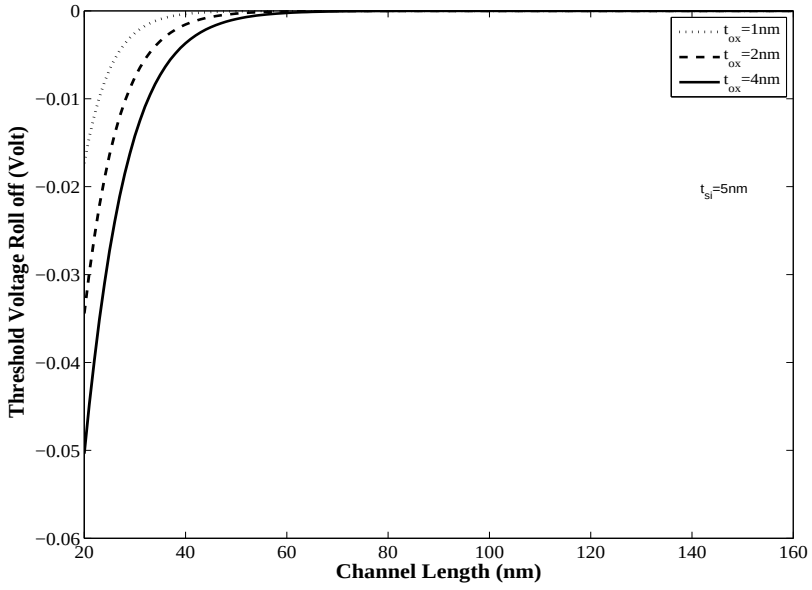

Figure 3.8: Threshold Voltage Roll-off of DGMOSFET w.r.t Channel length for different t_{ox}

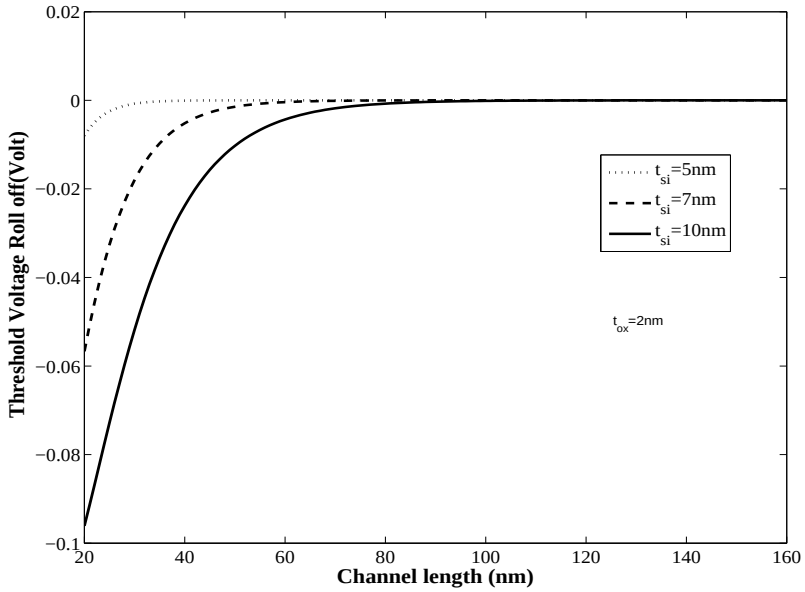

Figure 3.9: Threshold Voltage Roll-off of DGMOSFET w.r.t Channel length for different t_{si}

3.2.1.2 Drain Induced Barrier Lowering (DIBL)

DIBL is a secondary effect in MOSFETs referring originally to a reduction of threshold voltage of the transistor at higher drain voltage. The combined charge in the depletion region of the device and that in the channel of the device is balanced by three electrostatic charges: the gate, the source and the drain. As the drain voltage is increased, the depletion region of the pn-junction between the drain and the body increases in size and extends under the gate. So, the drain assumes a greater portion of the burden of balancing depletion region charge, leaving a smaller burden for the gate. As a result, the charge present near the gate retains charge balance by attracting more carriers into the channel. It lowers the threshold voltage of the device. For this effect, the channel becomes more attractive for electrons. In other words, the potential energy barriers for electrons in the channel are lowered. Hence, the term barrier lowering is used to describe these phenomena. Barrier lowering increases as channel length is reduced.

The DIBL effect is defined as the decrease in threshold voltage when the drain voltage is increased from a low value $V_{d,low}$ to a high value $V_{d,high}$. This effect results in lowering of the source/silicon potential barrier after application of a high drain voltage, leading to reduction of the threshold voltage and at the end to lack of the gate control. The DIBL effect occurs

when the barrier height for channel carriers at the edge of the source is reduced due to the influence of the drain electric field, upon application of a high drain voltage. If the barrier between the source and the channel is decreased, electrons are more freely injected into the channel region. Therefore, the threshold voltage is lowered and the gate has less control on the channel. The DIBL effect can be extracted from the analytical model[32].

$$DIBL = B[Z]^{1/2}\left\{[Z+V_{d,high}]^{1/2}-[Z+V_{d,low}]^{1/2}\right\}-C\left(V_{d,high}-V_{d,low}\right) \tag{3.30}$$

where $Z = V_{bi} - V_{thermal}\ln\left(\frac{Q_{th}}{n_i t_{si}}\right)$,
$B = \frac{2\exp\left(\frac{L}{2\lambda}\right)\left(1+\exp\left(\frac{L}{\lambda}\right)\right)}{\left(\exp\left(\frac{L}{\lambda}\right)-1\right)^2}$,
$C = \frac{2\exp\left(\frac{3L}{\lambda}\right)-4\exp\left(\frac{2L}{\lambda}\right)+2\exp\left(\frac{L}{\lambda}\right)}{\left(\exp\left(\frac{L}{\lambda}\right)-1\right)^4}$,
$\lambda\left(\frac{t_{si}}{4}\right) = \sqrt{\frac{\varepsilon_{si}t_{ox}t_{si}}{2\varepsilon_{ox}}\left(1+\frac{\varepsilon_{ox}t_{si}}{4\varepsilon_{si}t_{ox}}-\frac{\varepsilon_{ox}t_{si}^2}{16\varepsilon_{si}t_{ox}t_{si}}\right)}$.

The variation of DIBL is shown in the Fig. 3.10 with respect to channel length for $t_{ox} = 2nm$ and $t_{si} = 5nm$. From the Fig. 3.10, it is observed that as the channel length increases, the DIBL decreases. Our purpose is also to optimize the DIBL with two design parameters t_{ox} and t_{si}. So the study of variation of DIBL with respect to the channel length has been done for different values of t_{ox} and t_{si}.

In the Fig.3.11, the analysis of DIBL has been shown with respect to length of the channel for three different value of t_{ox} = 1nm, 2nm and 4nm, at $t_{si} = 5nm$. In Fig. 3.12, the analysis has been done for three values of t_{si} = 5nm, 7nm and 10nm and $t_{ox} = 2nm$. From the analysis of the figures, it has been seen that the DIBL is more severe as the thickness of the silicon body (t_{si}) and oxide layer (t_{ox}) decreases due to short channel effects. It is clearly seen that the DIBL effect becomes more prominent with shrinking the channel length below 30nm, with the DIBL effect becoming less severe for thinner silicon films due to the better gate control of the channel.

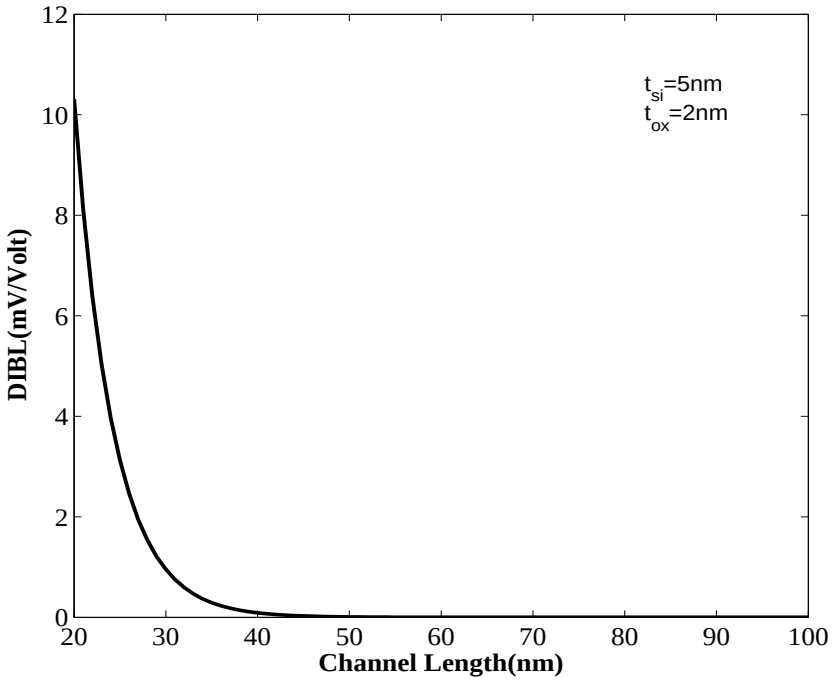

Figure 3.10: DIBL of DGMOSFET w.r.t Channel length

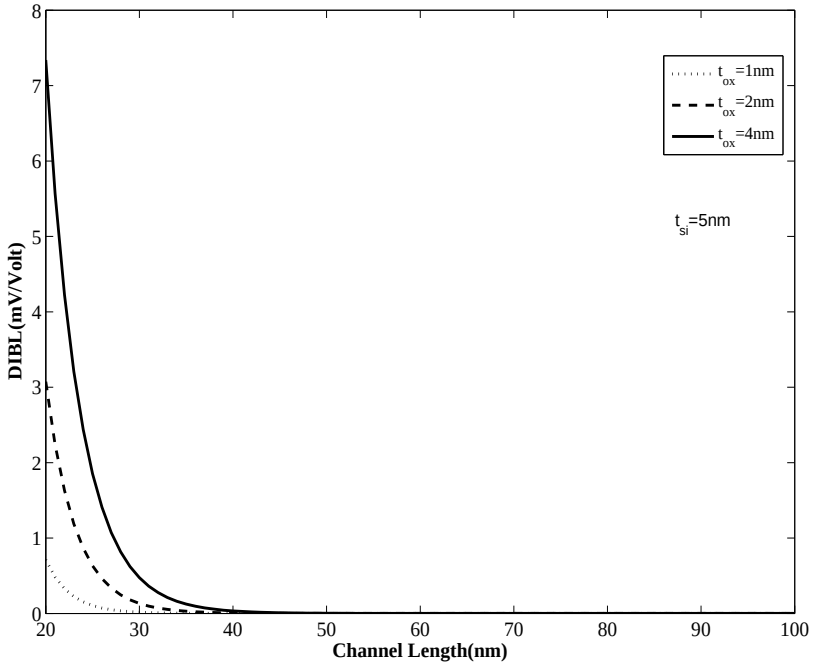

Figure 3.11: DIBL of DGMOSFET w.r.t Channel length for different t_{ox}

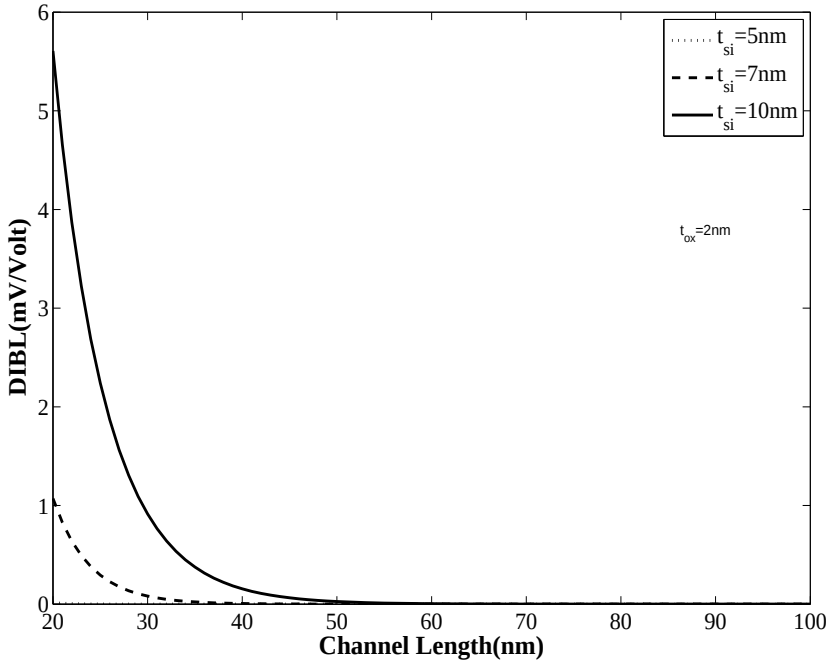

Figure 3.12: DIBL of DGMOSFET w.r.t Channel length for different t_{si}

3.2.1.3 Subthreshold Swing (SS)

In a MOSFET, the minimum voltage swing is required to turn on the transistor. The voltage swing is a very important factor because it ultimately set the minimum power supply voltages and minimum power dissipation of a device. The sub-threshold swing is defined as the gate voltage required to change the drain current by one order of magnitude per decade. The expression for sub-threshold swing is

$$SS = \left(1 - 2\Gamma_1 \cos\left(\frac{t_{si}}{4\lambda_1}\right) \exp\left(-\frac{L}{2\lambda_1}\right)\right)^{-1} \frac{KT}{q} \ln 10, \tag{3.31}$$

where $\Gamma_1 = \left(\frac{\frac{2\lambda_i}{t_{si}} \sqrt{\left(1+\frac{t_{si}^2}{r^2\lambda_i^2}\right)}}{\left(\frac{1}{r}+\frac{1}{2}+\frac{1}{2}\frac{t_{si}^2}{r^2\lambda_i^2}\right)} \right)$ and $r = \frac{\varepsilon_{ox} t_{si}}{\varepsilon_{si} t_{ox}}$.

with a condition

$\lambda_1 = \left(\frac{1+{}^{1}\!/_{r}}{1+{}^{\pi}\!/_{2}}\right) t_{si}, r \leq \frac{\pi}{2}$,

$\lambda_1 = \left(\frac{1+{}^{\sqrt{2}}\!/_{r}}{\sqrt{2}+{}^{\pi}\!/_{2}}\right) t_{si}, r \leq \frac{\pi}{2}$

In MOSFET, the sub-threshold swing is limited to $\frac{KT}{q}\ln 10$ [36] or 60 mV/decade at room temperature 300K. With scaling, it has been seen that the sub-threshold swing increases [37]. As the gate length deceases, the SS increases, which is the limitation of a MOSFET. The main approach is to optimize the value of Sub-threshold slope to get proper value of SS for which the device gives the better performance.

The Fig. 3.13 shows the variation of Sub-threshold Swing (SS) with respect to channel length varying from 20nm to 100nm. It shows that for values of $L > 40nm$, the sub-threshold slope approaches to its ideal value of $\frac{KT}{q}\ln 10$ i.e about 60mV/decade. The variation of Sub-threshold Swing is shown in the Fig. 3.13 with respect to channel length for $t_{ox} = 2nm$ and $t_{si} = 5nm$. It is observed that as the channel length increases, the Sub-threshold Swing decreases and then saturates at 60mV/decade. So, the study of variation of Sub-threshold Swing with respect to the channel length has been analyzed for different values of t_{ox} and t_{si}.

In the Fig. 3.14, the analysis of Sub-threshold Swing is shown with respect to length of the channel for three different value of t_{ox}=1nm, 2nm and 4nm, at $t_{si} = 5nm$. In Fig. 3.15, the analysis has been done for three values of $t_{si} = 5nm$, 7nm and 10nm and $t_{ox} = 2nm$. From the analysis of the figures, it has been seen that the SS decreases as the thickness of the silicon body (t_{si}) and oxide layer (t_{ox}) decreases. At lower channel length, the SS becomes more than 60mv/decade.

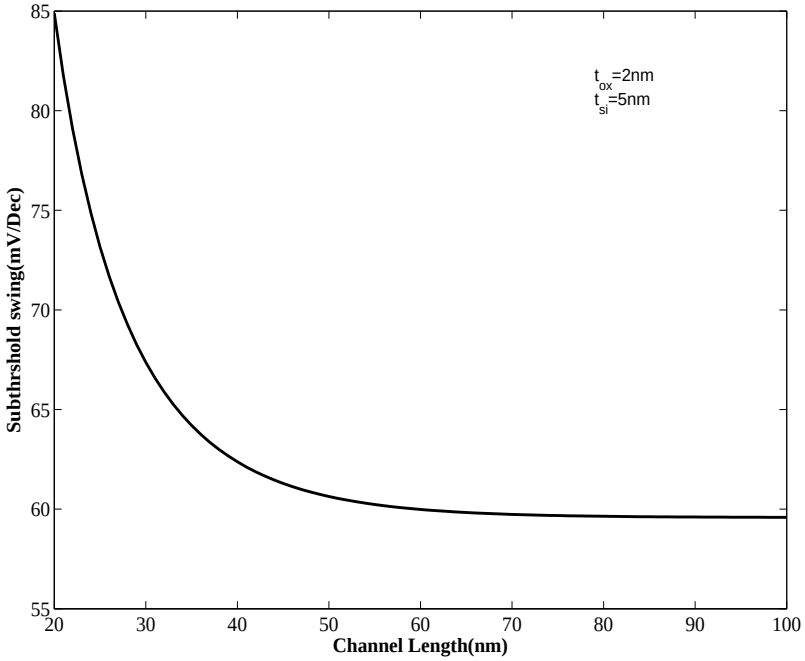

Figure 3.13: Subthreshold Swing w.r.t Channel length

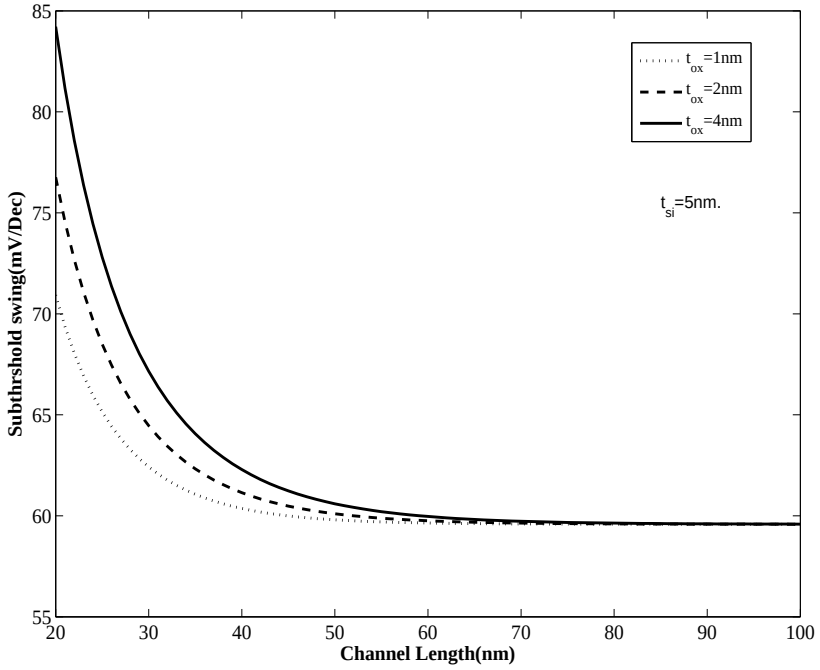

Figure 3.14: Subthreshold Swing w.r.t Channel length for different t_{ox}

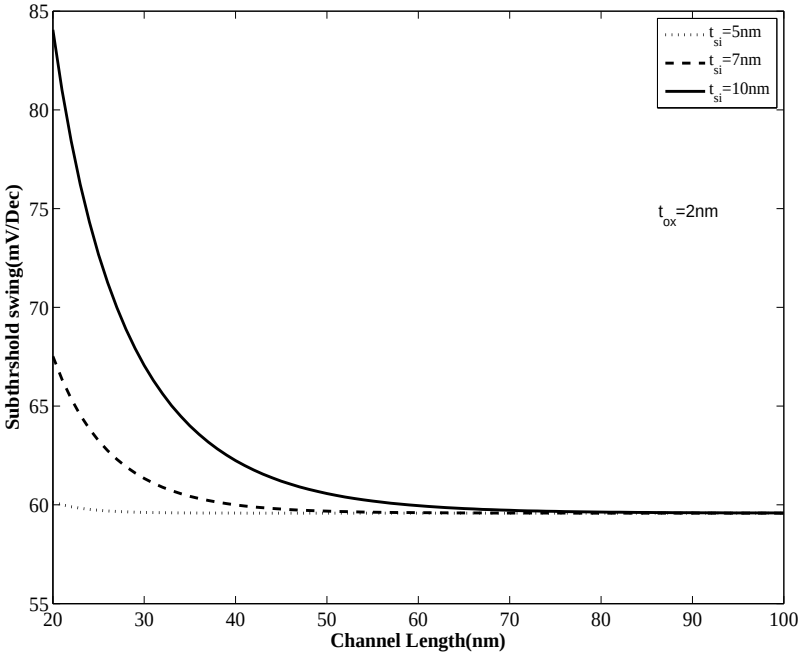

Figure 3.15: Subthreshold Swing w.r.t Channel length for different t_{si}

3.3 Summary

- This Chapter contributes a study of drain current model of a symmetrical DG MOSFET [28, 29, 31].
- The variation of electric potential with respect to position in channel for different values of β is observed. This signifies that as the β values decreases the bending becomes lesser.
- The drain to source current is studied by changing drain to source voltage for different values of gate voltage.
- By using the model [31], one of the important SCEs, i.e. Velocity Saturation is derived. The effect of drain current due to velocity saturation is studied.
- The velocity saturation increases with increase in gate potential. After certain voltage, it saturates to a constant value.
- Then, another modeling i.e. Threshold Voltage model is used [32] to derive different SCEs such as ΔV_{th}, DIBL and SS.

- The ΔV_{th} increases with decrease in gate length and in increase in t_{si} and t_{ox}.
- DIBL becomes more prominent with shortening the channel length below 40nm and less severe with shortening the thickness of channel and oxide layer.
- Subthreshold Swing has been derived from the device characteristics. The SS approaches its ideal value, $\frac{KT}{q}\log 10$ i.e. 60mv/dec, for channel length grater than 40nm. As t_{si} and t_{ox} decreases, the SS approaches to 60 mv/dec.

CHAPTER 4

Performance Analysis based on Channel Engineering

In the Previous Chapters, threshold and current modeling are discussed to get a overview on the effect of different design parameters of the DG MOSFET on SCEs. Performance analysis of the Device has been carried out by the MATLAB software. To validate the characteristics of the short channel effects and to improve the performance of the device, a user friendly device simulator ATLAS is used. For the improvement of the performance, a channel engineering technique may be used. Further to reduce the short channel effects, a study is carried out by changing the S/D region.

4.1 Introduction:

The schematic structure of the DG MOSFET is shown in the Fig. 2.1 in the Chapter 2. The supply voltage V_g is given to both front and back gates. Here, three different gate lengths 40nm, 20nm and 10nm are considered for analysis and the length of the source and drain is considered to be 20nm. The thickness of the silicon channel and oxide layer are taken as 5nm and 2nm respectively. The device dimensions are given in the Table 4.1 below. Also the schematic diagram of the device for $L = 20nm$ after simulation in ATLAS simulator has been given in Fig. 4.1 below. To enhance the performance and to reduce the SCEs of the device, the channel has been lightly doped [39].

Table 4.1: Dimensions and doping concentrations for device

Attributes	Value
L	40nm, 20nm and 10nm
t_{si}	5nm
t_{ox}	2nm
N_A(Channel doping)	$10^{16}cm^{-3}$
N_S(Source doping)	$10^{20}cm^{-3}$
N_D(Drain doping)	$10^{20}cm^{-3}$

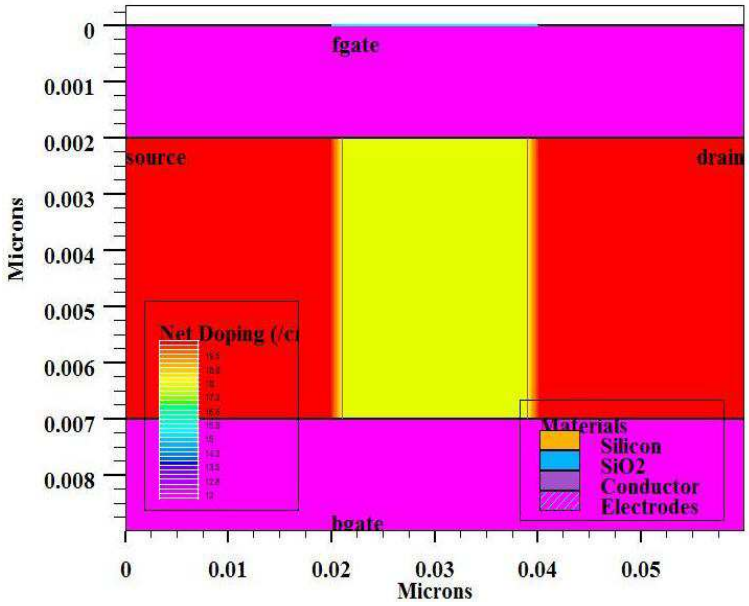

Figure 4.1: Schematic Diagram for $L = 20nm, t_{si} = 5nm$ and $t_{ox} = 2nm$

4.2 Performance Analysis

For performance enhancement and reduction of the SCEs, different structures are considered in this section. The performance and behavior of the device are studied by varying the L, t_{si}, t_{ox} [41]. A step is made to improve the performance and reduce the SCEs by taking different combinations of these above design parameters.

The transfer characteristics, i.e. $I_{ds} \quad vs \quad V_{gs}$ for different V_{ds} are shown in the Fig. 4.2 and Fig. 4.3 by varying L, t_{si}. Here for two different values of V_{ds}, i.e. 0.1 volt and 1 volt, the $I_{ds} \quad vs \quad V_{gs}$ is studied. The Fig. 4.2 shows that the drain current increases with decrease in channel length, which decreases the intrinsic gain of the device and hence degrades the performance. Similarly, Fig. 4.3 shows the characteristics for three different silicon channel thickness. It shows that the drain current increases with increase in channel thickness.

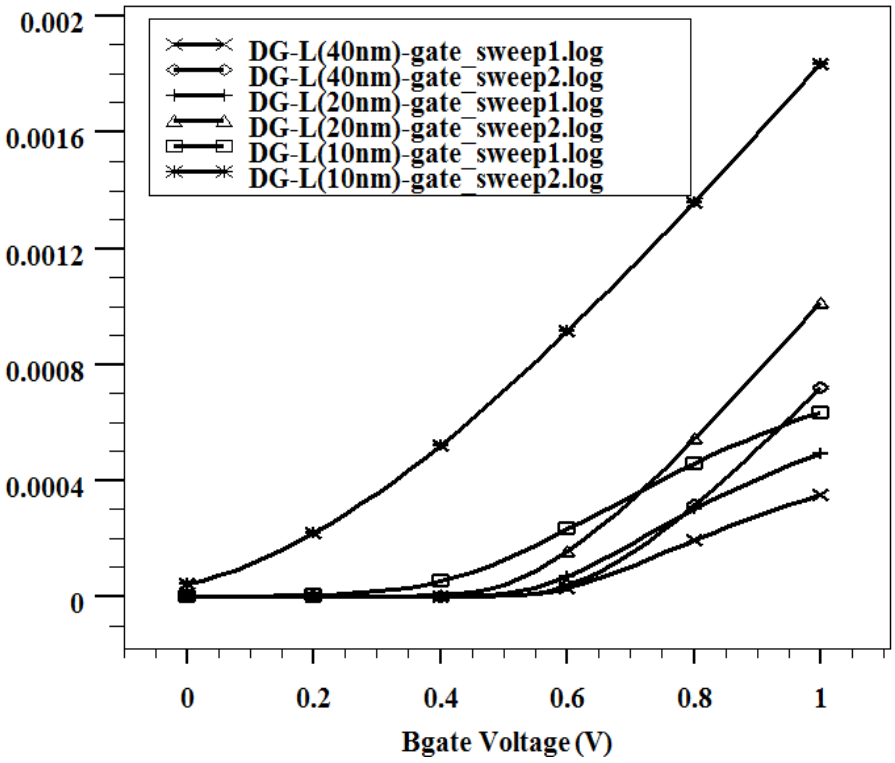

Figure 4.2: I_d vs V_g curve by varying L (10nm, 20nm and 40nm)

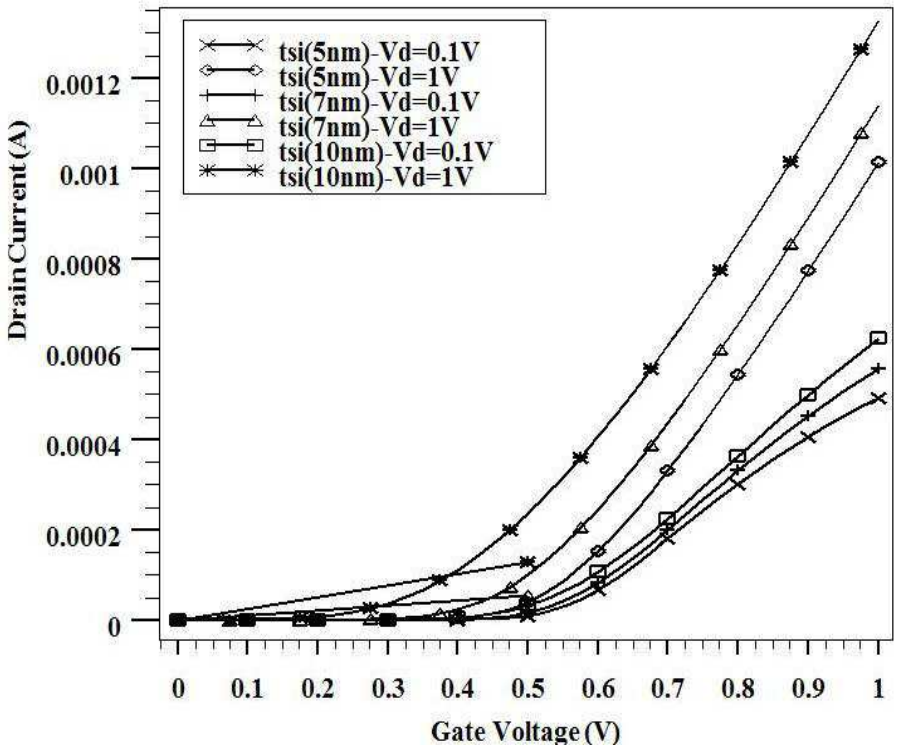

Figure 4.3: I_d vs V_g curve by varying t_{si} (5nm, 7nm and 10nm)

The parameters like Threshold voltage, Sub threshold Swing, Transcoductance, DIBL, I_{on} and I_{off} are extracted by using ATLAS device simulator. These results have been compared with the results of analytical model to validate the model.

4.2.1 Threshold Voltage

From the simulation, it has been seen that the threshold voltage reduces as the length of the channel is shorten. Therefore, a small amount of gate voltage is required to switch on the device which is harmful for the device and the maximum drain current (I_{on}) increases. It has also been observed that as we are reducing the t_{si}, V_{th} increases. The Fig. 4.4 shows the variation of Threshold voltage with respect to L, t_{si} and t_{ox}.

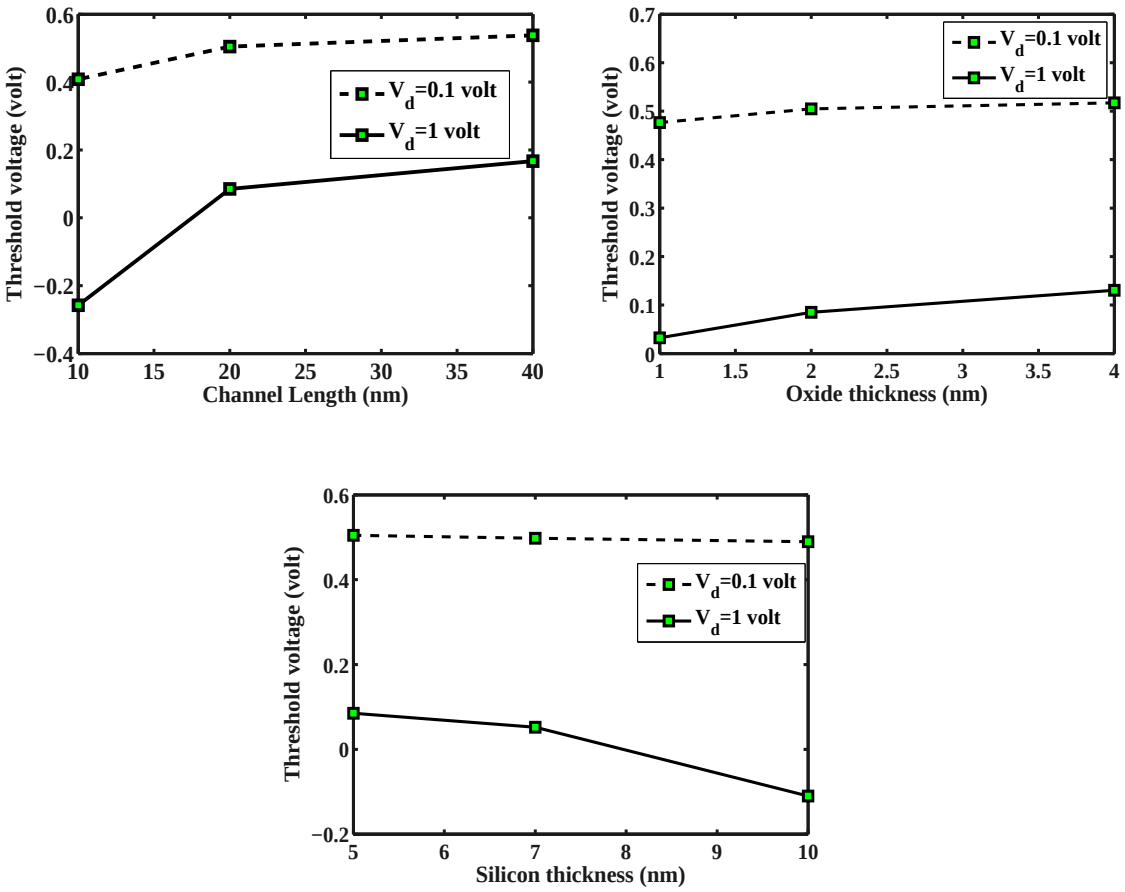

Figure 4.4: Variation of V_{th} as a function of L, t_{si} and t_{ox}

4.2.2 Subthreshold Leakage Current

From the Fig. 4.5, it shows the variation of sub-threshold leakage current with respect to L, t_{si} and t_{ox}. As the length of the gate decreases, the subthreshold leakage current increases and also the control of the gate on leakage current decreases. Therefore, the sub-threshold leakage current is higher at lower device channel length. For the devices with higher silicon channel thickness there will be a increase in sub-threshold current and decrease in threshold voltage (V_{th}), due to weak channel electrostatics. As the gate oxide thickness decreases from 4 to 1 nm, keeping other parameters constant ($t_{si} = 5nm,\ L = 20nm,\ V_d = 0.1V\ and\ 1.0V$) then the sub-threshold current decreases 100 or 1000 folds. It is because, thicker gate oxide,

gate characteristics get weakens in the channel which results in some loss of control over the channel and this increases sub-threshold current.

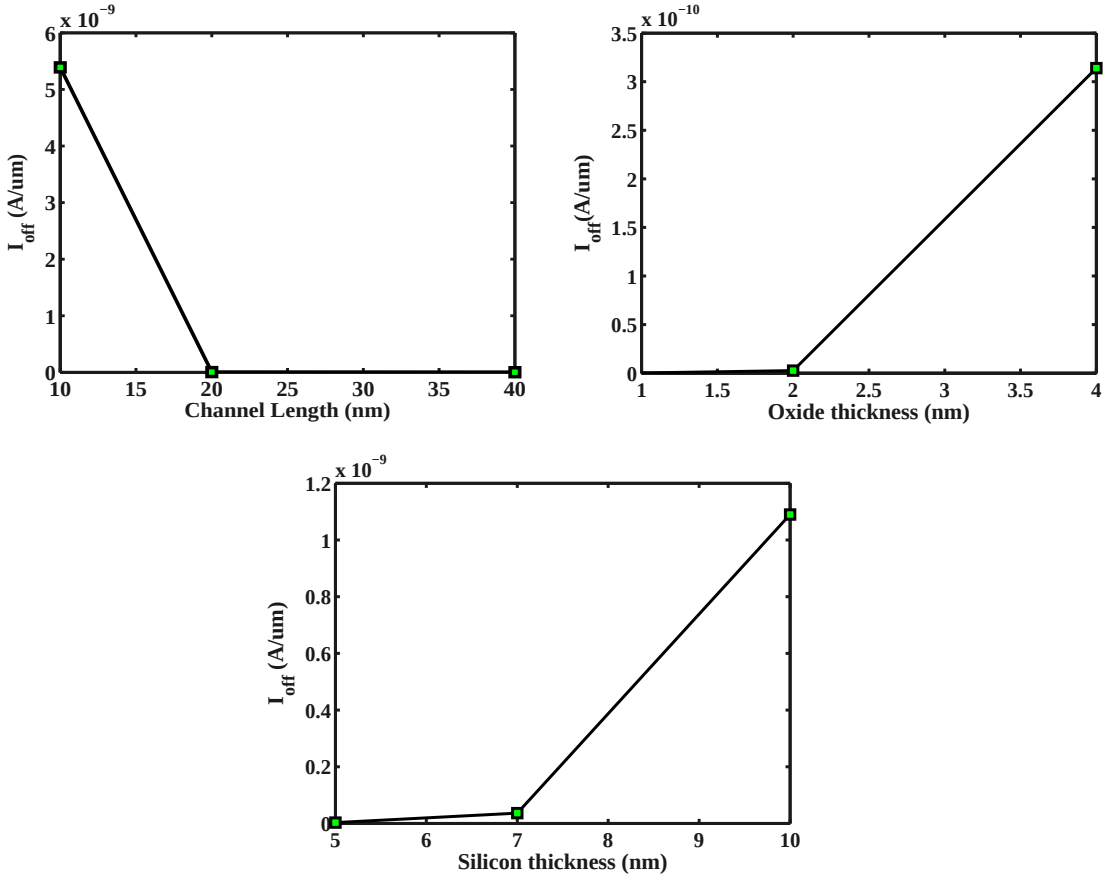

Figure 4.5: Variation of Leakage Current(I_{off}) as a function of L, t_{si} and t_{ox}

4.2.3 Subthreshold Swing

The sub-threshold swing with respect to change in L, t_{ox} and t_{si} is shown in the Fig. 4.6. It has been seen clearly that for shorter channel length, SS increases because of the enhanced control of the drain over the channel changes. From Fig. 4.6, as the thickness of the silicon channel increases, the SS increases rapidly and as thickness of the gate oxide increases, the SS parameter increases.

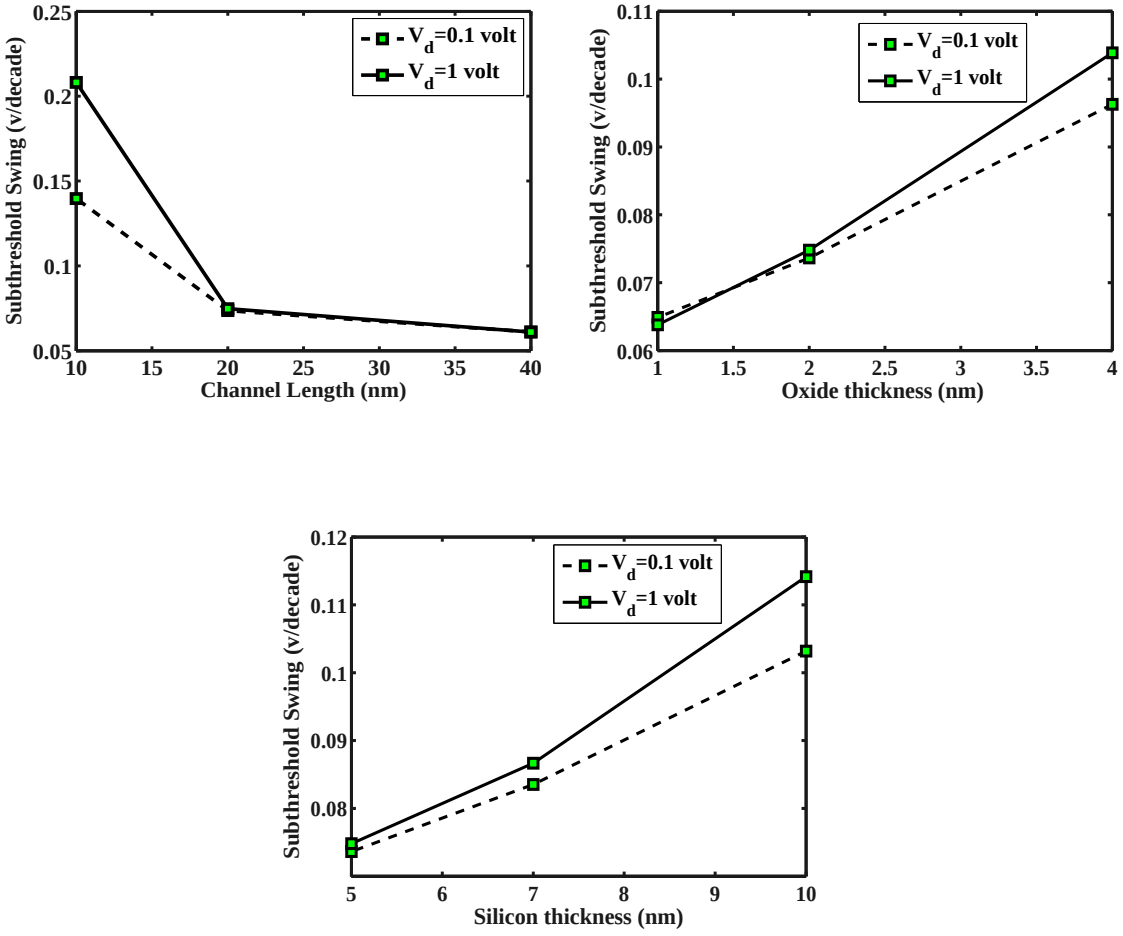

Figure 4.6: Effect of Subthreshold Swing with the variation of L, t_{ox} and t_{si}

4.2.4 Drain Induced Barrier Lowering

The DIBL is one of the SCEs. This effect results in lowering the source or silicon potential barrier after application of a high drain voltage, leading to reduction of the threshold voltage and also reduces the gate control. The variation of DIBL with respect to L, t_{si} and t_{ox} is shown in the Figure below with $V_d = 0.1V\, and\, 1V$ respectively. The DIBL increases as, we reduce the channel length with $t_{si} = 5nm$, $t_{ox} = 2nm$, which is shown in Fig. 4.7. The Fig. 4.7 demonstrates the change in DIBL with respect to change in t_{si} with $L = 20nm$, $t_{ox} = 2nm$. It is seen that the DIBL becomes less severe for thinner silicon films.

The DIBL can also be reduced by thickening the gate oxide layer, which has been observed from Fig. 4.7.

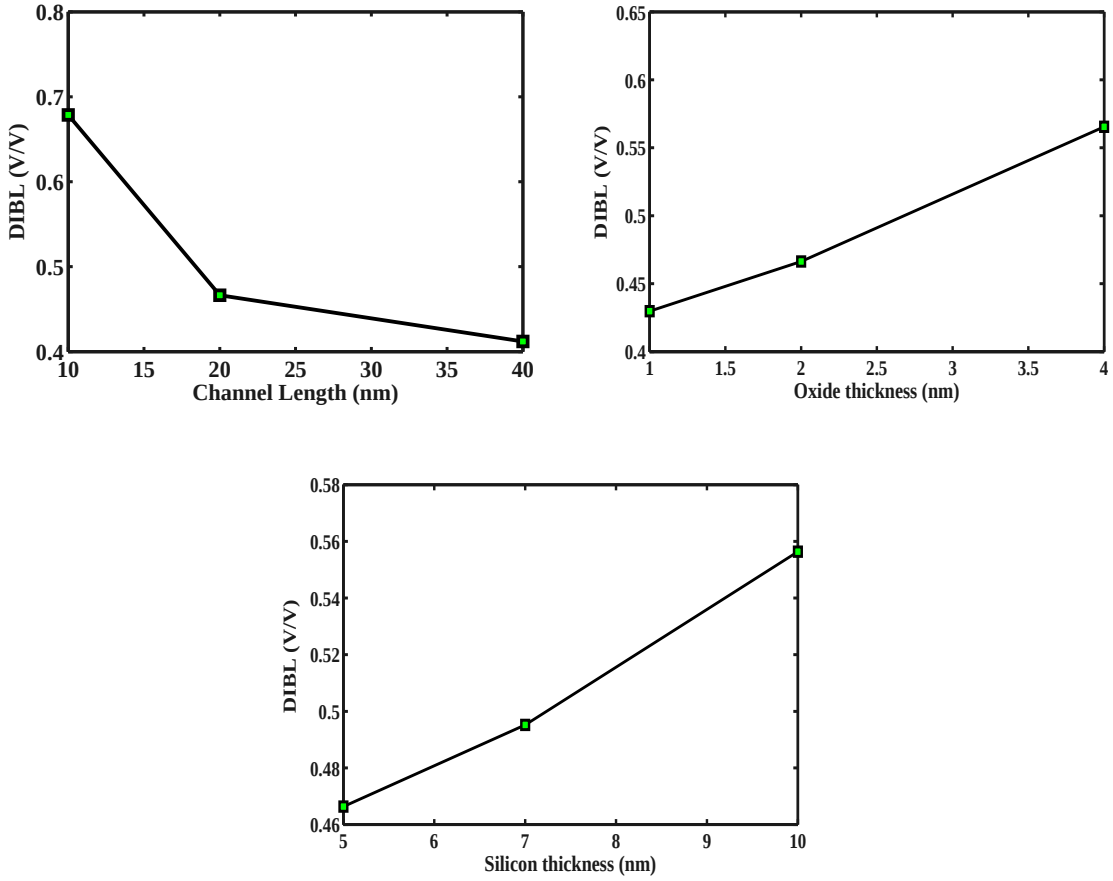

Figure 4.7: DIBL with the variation of L,t_{si} and t_{ox}

4.2.5 Maximum Drain Current

The variation of maximum drain current (I_{on}) has been studied. Fig. 4.8 shows the I_{on} as the function of L, t_{si} and t_{ox} at V_d =0.1V and 1V . The Figures show that I_{on} increases with decrease in the length of the channel (L) and thickness of $SiO_2(t_{ox})$ and decreases with the decrease in thickness of the silicon channel (t_{si}).

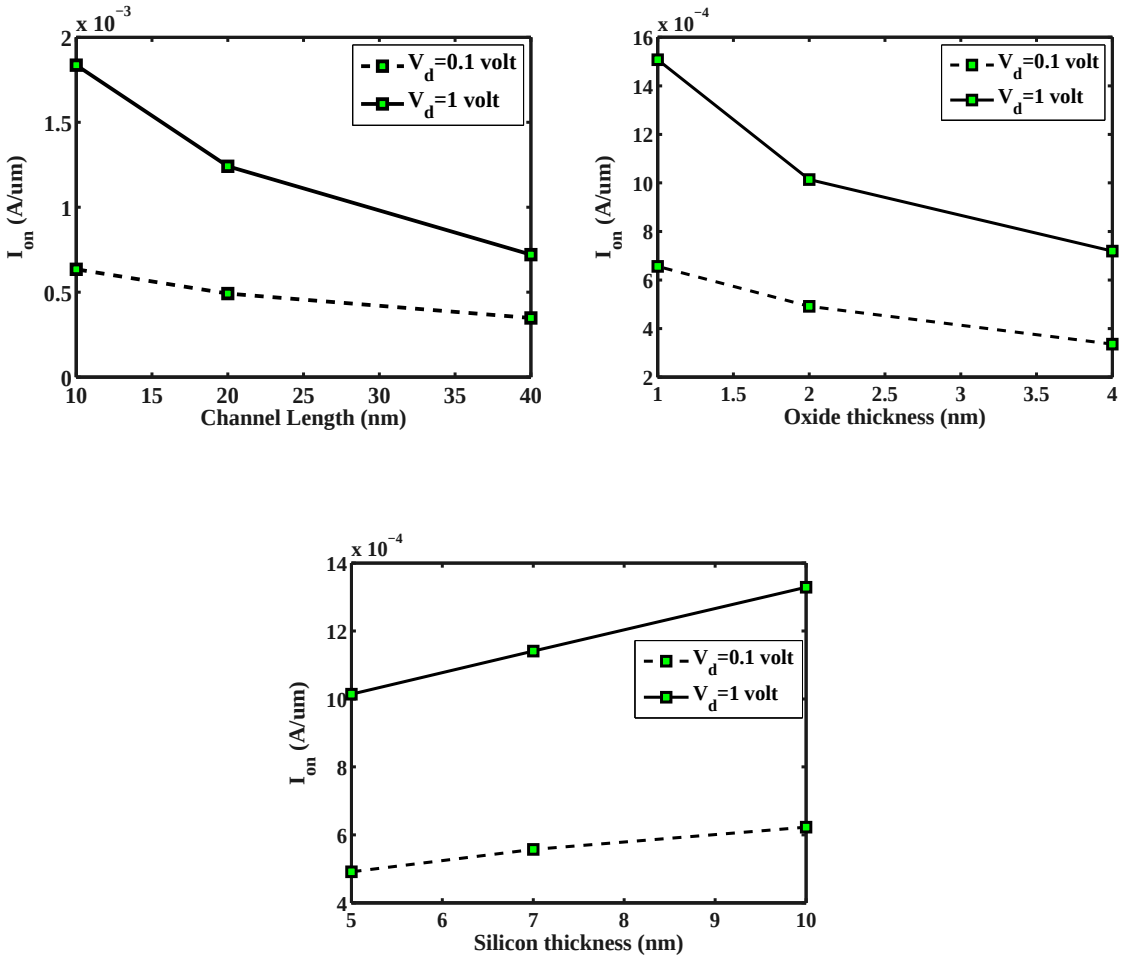

Figure 4.8: Behavior of I_{on} with respect to L, t_{si} and t_{ox}

4.2.6 Transconductance

The extraction value of transconductance (g_m) shows that it is increasing with shorter channel lengths and thinner oxide layer which is good for high performance circuit requirements. Fig. 4.9 shows that g_m increases with decrease in L and t_{ox} but decreases with increase in t_{si}.

The Table 4.2-4.4 shows the parameter extraction with respect to change in L, t_{si} and t_{ox}.

4.2.7 Observation

The SS and DIBL increases with reducing the channel length or increasing channel thickness and oxide thickness. The threshold voltage decreases as the channel length is reduced. Various results have been discussed from various structures by changing L, t_{si} and t_{ox} . The V_{th} should not be very low or not too high. If V_{th} will be very low, it will the switch on the device very quickly and if it is very high then it will reduce the I_{on} hence increases the speed of the circuit. Therefore, from the analysis we have got the device having the structure $L = 20nm$, $t_{si} = 5nm$, $t_{ox} = 2nm$ provides good value of V_{th} for which the I_{on} is high and I_{off} is very low, DIBL is also low, g_m is high and SS is of 73 mv/decade. The main objective is to reduce the SCEs (DIBL, I_{off}, and SS) further to get better performance of the device.

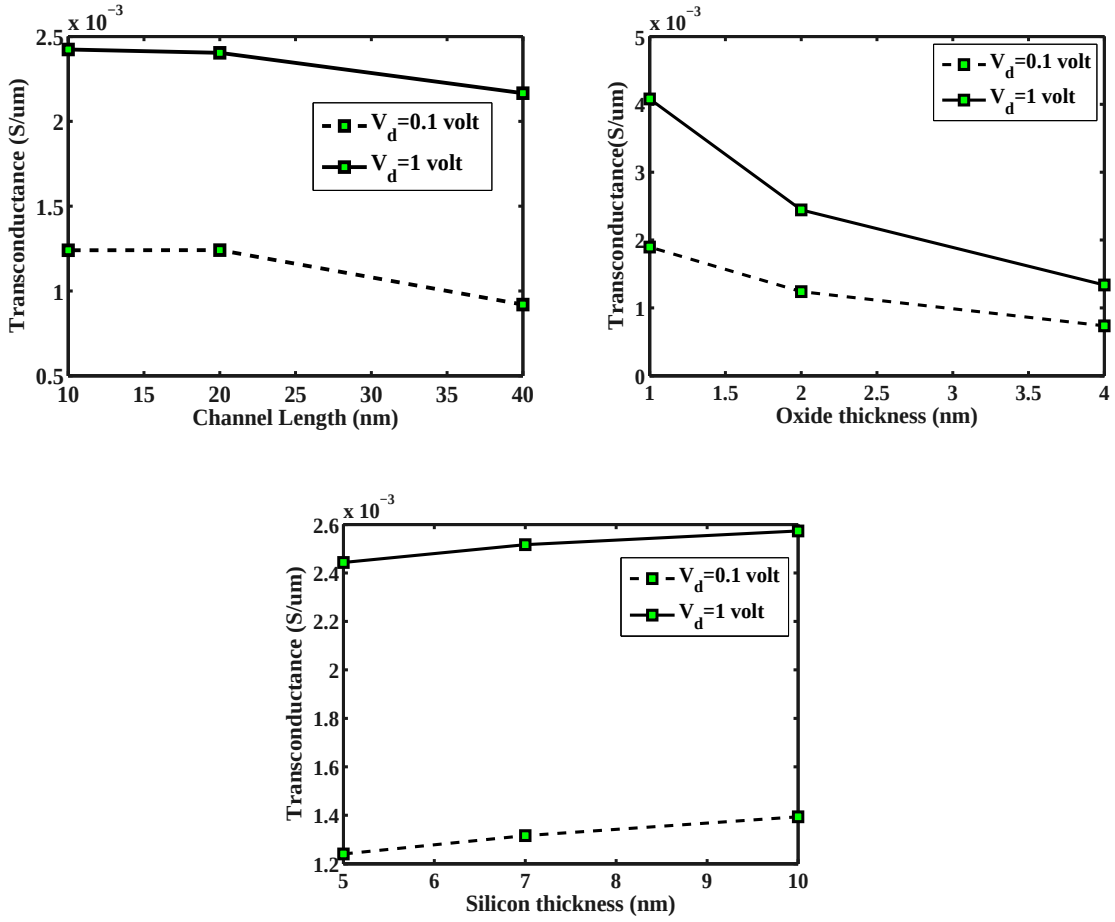

Figure 4.9: Effect of Transconductance (g_m) with respect to L, t_{si} and t_{ox}

Table 4.2: Extracted Parameters from $I_d - V_g$ and $I_d - V_d$ curve for varying L [41]

Varying L			
T_{si}=5nm.,T_{ox}=2nm.,V_d=0.1v			
	L=40nm	L=20nm	L=10nm
V_{th}(V)	0.537842	0.504721	0.408322
SS(V/decade)	0.0611069	0.0736342	0.1396641
$g_m(S/\mu m)$	0.00091958	0.00124041	0.00169762
I_{on}(A)	0.00034785	0.00049141	0.00063424
T_{si}=5nm,T_{ox}=2nm.,V_d=1v			
V_{th}(V)	0.167106	0.085007	-0.257683
SS(V/decade)	0.0610019	0.0748001	0.2081692
$g_m(S/\mu m)$	0.00216568	0.00244348	0.00242346
I_{on}(A)	0.00072094	0.00124041	0.00183634
I_{off}(A)	1.73E-13	2.64E-12	5.39E-09
DIBL(V/V)	0.411929	0.466347	0.678637

Table 4.3: Extracted Parameters from $I_d - V_g$ and $I_d - V_d$ curve for varying T_{si} [41]

Varying T_{si}			
L=20nm.,T_{ox}=2nm,V_d=0.1v			
	T_{si}=10nm	T_{si}=7nm	T_{si}=5nm
V_{th}(V)	0.489713	0.497814	0.50472
SS(V/decade)	0.103183	0.0835215	0.073634
$g_m(S/\mu m)$	0.001394	0.00131586	0.00124
I_{on}(A)	0.000623	0.00055735	0.000491
L=20nm,T_{ox}=2nm.,V_d=1v			
V_{th}(V)	-0.11025	0.0521175	0.085008
SS(V/decade)	0.114158	0.0748001	0.0748
$g_m(S/\mu m)$	0.002573	0.00251686	0.002443
I_{on}(A)	0.001329	0.00114074	0.001014
I_{off}(A)	1.09E-09	3.63E-11	2.64E-12
DIBL(V/V)	0.556375	0.495218	0.466347

Table 4.4: Extracted Parameters from $I_d - V_g$ and $I_d - V_d$ curve for varying T_{ox} [41]

Varying T_{ox}			
L=20nm.,T_{si}=5nm,V_d=0.1v			
	T_{ox}=4nm	T_{ox}=2nm	T_{ox}=1nm
V_{th}(V)	0.476593	0.50472	0.51725
SS(V/decade)	0.096287	0.073634	0.06488
$g_m(S/\mu m)$	0.000735	0.00124	0.00189
I_{on}(A)	0.000336	0.000491	0.00065
L=20nm,T_{si}=5nm.,V_d=1v			
V_{th}(V)	0.000336	0.085008	0.13044
SS(V/decade)	0.103875	0.0748	0.06378
$g_m(S/\mu m)$	0.001337	0.002443	0.00407
I_{on}(A)	0.000719	0.001014	0.00150
I_{off}(A)	3.14E-10	2.64E-12	2.16E-13
DIBL(V/V)	0.565467	0.466347	0.42978

4.3 Graded Channel Engineering(GCE)

The sub-threshold swing for $L = 20nm$, $t_{si} = 5nm$, $t_{ox} = 2nm$ is 73 mv/decade and for $L = 10nm$, it is 139 mv/decade. To further reduce the SS and I_{off} and to give better performance with high on current (I_{on}), graded channel engineering is applied in the structure. Therefore, to reduce the SCEs, the graded channel engineering technique is used in this section. The doping of the channel has been taken as high-med-low. The simulations have been done for the device by changing the length. The device dimensions are given below in the Table 4.5. The schematic diagrams of the device is presented in the Fig. 4.10 and Fig. 4.11 for L equal to 10nm and 20nm respectively.

Table 4.5: Device dimensions and doping concentrations with channel engineering

Attributes	Value
L	40nm,20nm,10nm
t_{si}	5nm
t_{ox}	2nm
N_A(Channel Doping)	$1 \times 10^{19}\ cm^{-3}$
	$1 \times 10^{18}\ cm^{-3}$
	$1 \times 10^{17}\ cm^{-3}$
N_S(Source Doping)	$1 \times 10^{20}\ cm^{-3}$
N_D(Drain Doping)	$1 \times 10^{20}\ cm^{-3}$

The Schematic diagram of the device with Graded Channel after simulation in ATLAS device simulator is shown in Fig. 4.10-4.11 for L=10nm and 20nm respectively. The transfer characteristics of the device has been studied. It is presented in the Fig. 4.12. The values of different parameters without channel engineering [41] and with graded channel engineering are recorded in the Tables 4.6-4.7 and are compared with each other.

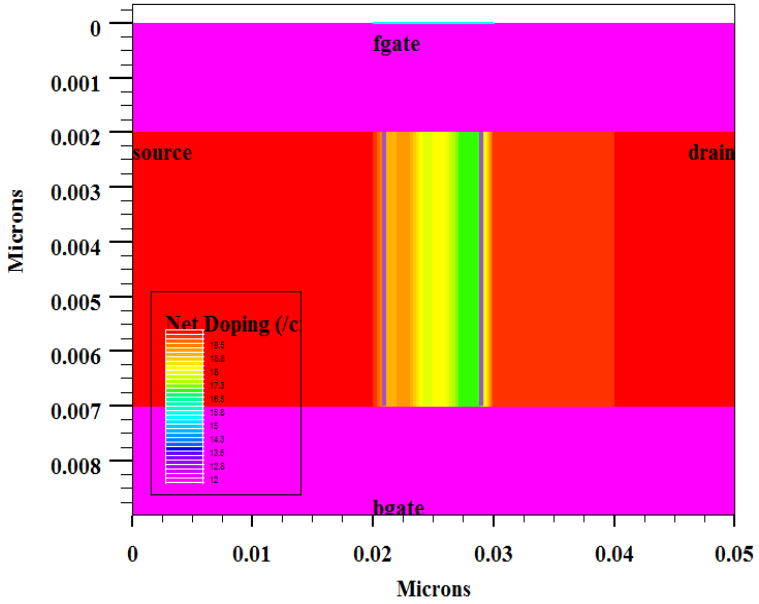

Figure 4.10: Schematic diagram of GC-DG-MOSFET with $L = 10nm$.

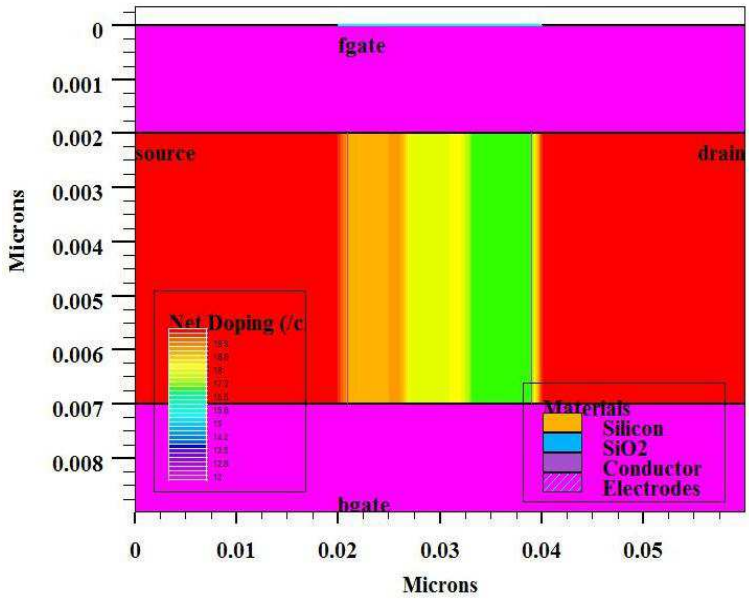

Figure 4.11: Schematic diagram of GC-DG-MOSFET with $L = 20nm$.

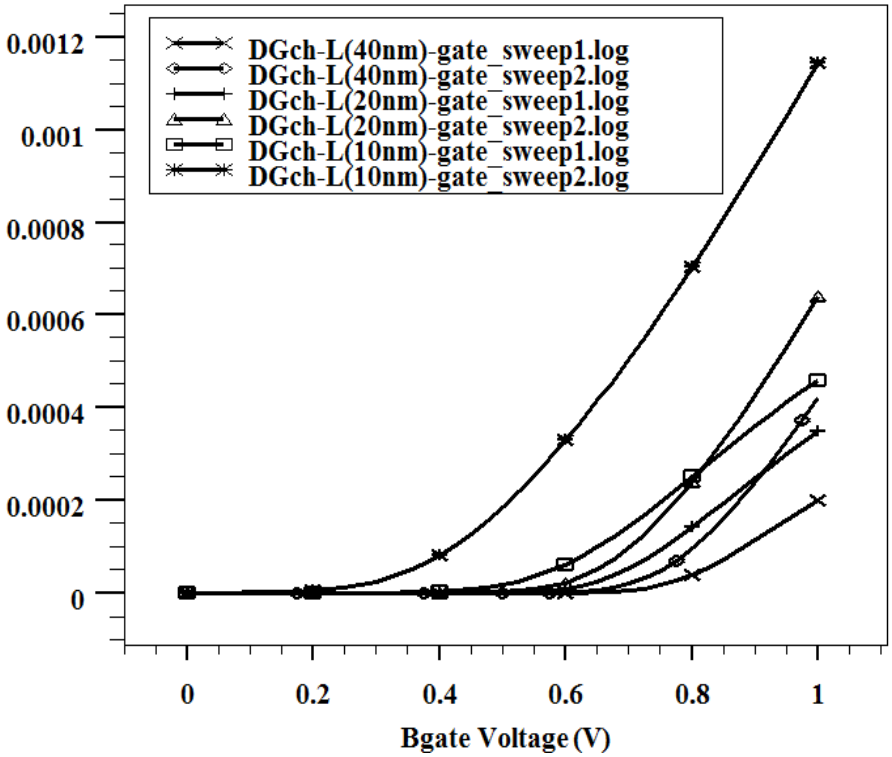

Figure 4.12: I_d vs V_g curve by varying L of GC-DG-MOSFET

Table 4.6: Extracted Parameters without Channel Engineering [41]

Without Channel Engineering			
T_{si}=5nm,T_{ox}=2nm,V_d=0.1v			
	L=40nm	L=20nm	L=10nm
V_{th}(V)	0.537842	0.50472	0.40832
SS(V/decade)	0.061107	0.073634	0.13966
$g_m(S/\mu m)$	0.00092	0.00124	0.00116
I_{on}(A)	0.000348	0.000491	0.00063
T_{si}=5nm,T_{ox}=2nm,V_d=1v			
V_{th}(V)	0.167106	0.085008	-0.25768
SS(V/decade)	0.061002	0.0748	0.20816
$g_m(S/\mu m)$	0.002166	0.002443	0.00242
I_{on}(A)	0.000721	0.00124	0.00183
I_{off}(A)	1.73E-13	2.64E-12	5.39E-09
DIBL(V/V)	0.411929	0.466347	0.67867

Table 4.7: Extracted Parameters with Channel Engineering

With Channel Engineering			
T_{si}=5nm,T_{ox}=2nm,V_d=0.1v			
	L=40nm	L=20nm	L=10nm
V_{th}(V)	0.718516	0.616992	0.50234
SS(V/decade)	0.0723154	0.075647	0.14177
$g_m(S/\mu m)$	0.000871	0.001067	0.00109
I_{on}(A)	0.0002	0.000348	0.00053
T_{si}=5nm,T_{ox}=2nm,V_d=1v			
V_{th}(V)	0.287345	0.208511	-0.15277
SS(V/decade)	0.070992	0.079906	0.17193
$g_m(S/\mu m)$	0.001941	0.002194	0.00231
I_{on}(A)	0.000423	0.000639	0.00151
I_{off}(A)	1.70E-13	5.56E-13	3.65397E-09
DIBL(V/V)	0.479079	0.453868	0.60659

The Fig. 4.13 shows the variation of parameters in graphical manner.

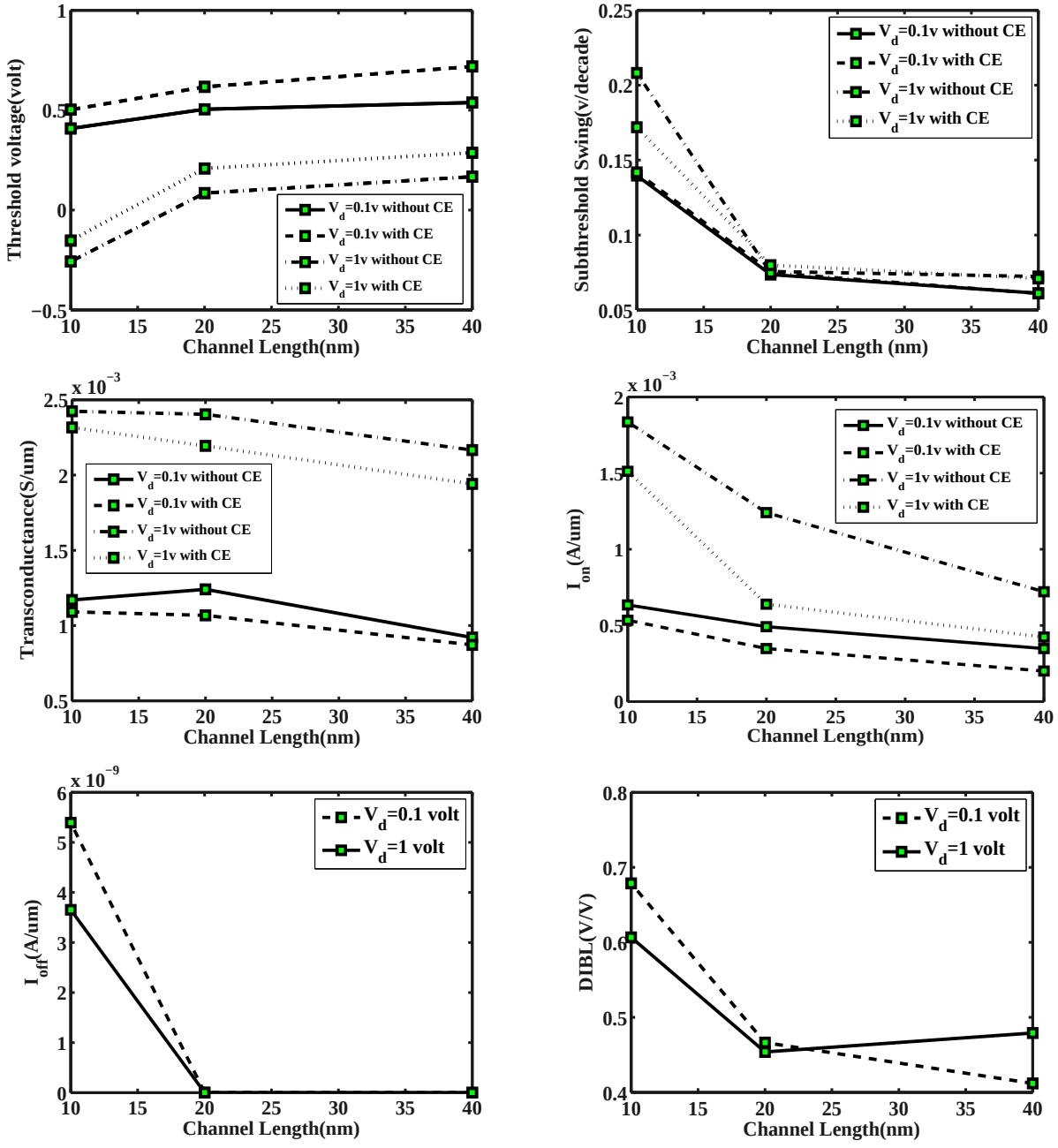

Figure 4.13: Effects of V_{th}, SS, g_m, I_{on}, I_{off} and DIBL with variation of L

4.3.1 Observation

The values of different parameters with GCE has been extracted and are compared with existing results [41] ,with out CE. It has been seen that with channel engineering technique, the leakage current decreases, which is good for the device but SS increases and V_{th} decreases which degrades the device performance. To obtain better performance, the SS should be equal to or nearly equal to 60mV/decade. Therefore GCE technique with changing doping concentration of S/D should be used.

4.4 GCE by changing the doping concentration of S/D region

The SS and I_{off} can also been reduced by changing the source and drain doping concentrations. From the Table 4.8, it has been seen that the SS and I_{off} are reduced further. The simulation and parameter extraction have been done by using ATLAS device simulator with the structure $t_{si} = 5nm$, $t_{ox} = 2nm$ and $N_{A,high} = 10^{19}$, $N_{A,med} = 10^{18}$, $N_{A,low} = 10^{17}$ by varying $L = 40nm$, $20nm$ and $10nm$ with varying N_S and N_D.

4.4.1 Observation

It has been observed that as the doping concentration is decreased, the device of all structures shows the better performance. The device having gate length 40nm gives good results of short channel effects. But from the analysis, it has been seen that the device also shows the good results for L=20nm and 10 nm also. By using Channel engineering with N_D=N_S=$0.25 \times 10^{20} cm^{-3}$, the SS is equal to 0.061 and 0.068 V/decade for L=20 and 10nm respectively. Where as without channel engineering, it was 0.073 and 0.112 V/decade respectively. Therefore, there is an increase in the SS parameter.

Similarly, the leakage current without CE has been recorded as $2.64 \times 10^{-12} cm^{-3}$ and $5.39 \times 10^{-09} cm^{-3}$ for $L = 20$ and 10nm respectively. The values recorded, after using Channel engineering with N_D=N_S=$0.25 \times 10^{20} cm^{-3}$ are equal to $5.14 \times 10^{-14} cm^{-3}$ and $1.123 \times 10^{-11} cm^{-3}$ respectively. Therefore, there is also an improvement of leakage current with CE followed by changing doping concentration.

The DIBL has been recorded without CE as 0.46 and 0.67V/V for $L = 20$ and 10 nm. respectively. But, there is decrease in DIBL of 0.42 and 0.47/V respectively with CE with N_D=N_S=$0.25 \times 10^{20} cm^{-3}$.

From the above study, it can be observed that the short channel effects like leakage current and SS can be reduced. Fig.4.14 shows the effect of SCE with respect to length of

the channel for different doping concentration of source and drain.

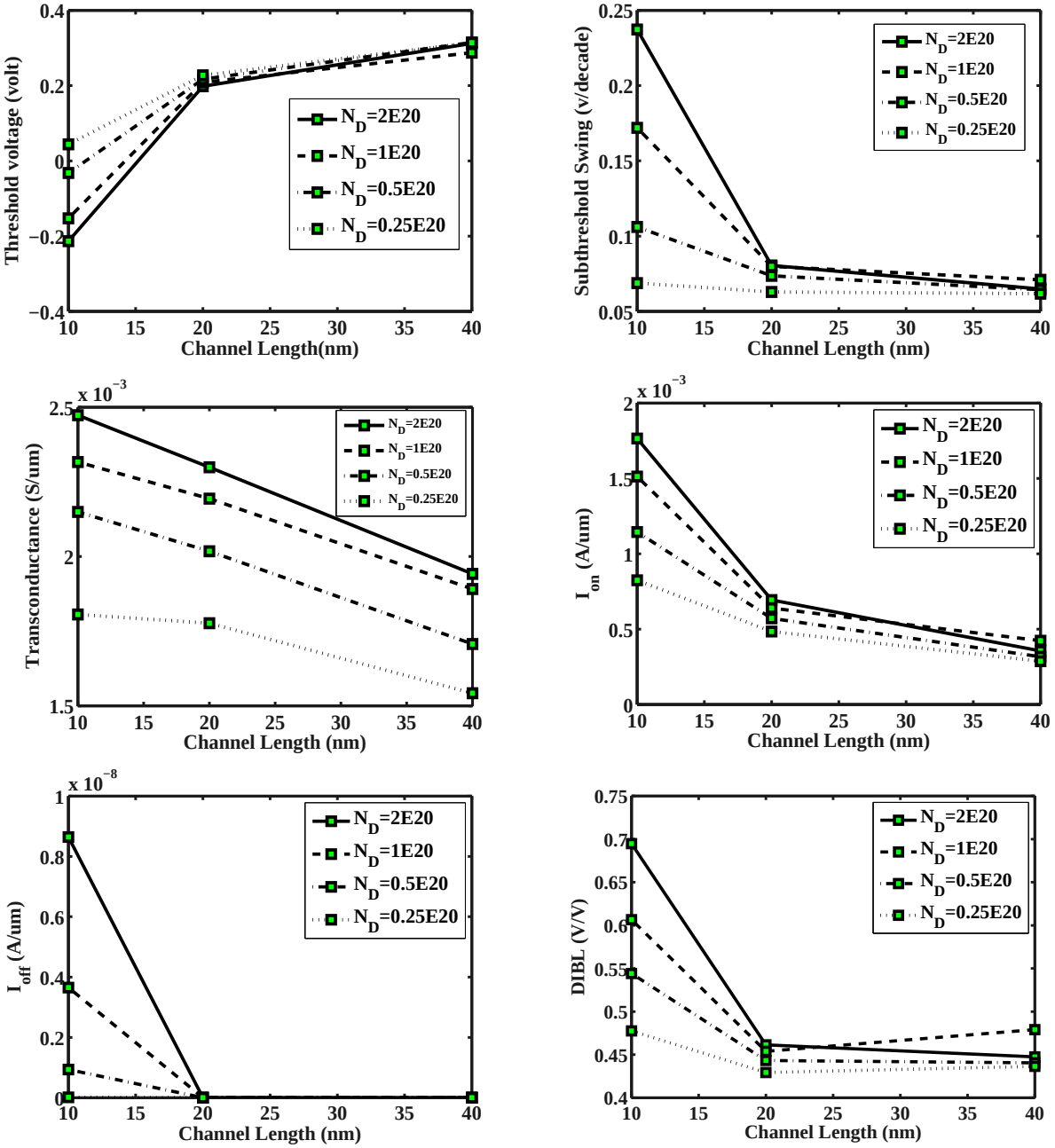

Figure 4.14: Effects of V_{th}, SS, g_m, I_{on}, I_{off} and DIBL for different S/D doping

Table 4.8: Comparison of extracted parameters by changing N_D

	T_{si}=5nm,T_{ox}=2nm,V_d=0.1v											
	$N_D = 2e20cm^{-3}$			$N_D = 1e20cm^{-3}$			$N_D = 0.5e20cm^{-3}$			$N_D = 0.25e20cm^{-3}$		
	L=40nm	L=20nm	L=10nm	L=40nm	L=20nm	L=10nm	L=40nm	L=20nm	L=10nm	L=40nm	L=20nm	L=10nm
V_t	0.71484	0.61378	0.49932	0.71851	0.61699	0.50235	0.71124	0.61599	0.51275	0.70696	0.61380	0.52371
SS	0.06478	0.07585	0.15078	0.07231	0.07564	0.14173	0.06443	0.07435	0.12183	0.06079	0.06156	0.06867
g_m	0.00089	0.00117	0.00121	0.00087	0.00106	0.00109	0.00075	0.00091	0.00091	0.00065	0.00075	0.00073
I_{on}	0.00020	0.00039	0.00063	0.00020	0.00034	0.00053	0.00017	0.00029	0.00041	0.00015	0.00023	0.00030
	T_{si}=5nm,T_{ox}=2nm,V_d=1v											
V_t	0.31213	0.19845	-0.2133	0.28734	0.20851	-0.1527	0.31473	0.21706	0.03212	0.31410	0.22746	0.04387
SS	0.06480	0.08045	0.23730	0.07099	0.07990	0.17193	0.06437	0.07357	0.10609	0.06180	0.06285	0.06880
g_m	0.00189	0.00229	0.00247	0.00194	0.00219	0.00231	0.00170	0.00201	0.00214	0.00150	0.00177	0.00180
I_{on}	0.00035	0.00069	0.00176	0.00042	0.00063	0.00151	0.00031	0.00057	0.00114	0.00030	0.00048	0.00082
I_{off}	7.6E-14	8.9E-13	8.6E-09	1.7E-13	5.5E-13	3.6E-09	7.4E-14	3.2E-13	9.3E-10	5.6E-15	5.1E-14	1.1E-11
DIBL	0.44745	0.46147	0.6947	0.47907	0.45386	0.60659	0.44056	0.44325	0.54410	0.43651	0.42926	0.47753

4.5 Conclusion

- The transfer characteristics has been studied for $V_d = 0.1V$ and $1V$ by varying L and t_{si}. The drain current increases with decrease in channel length and with increase in channel thickness.

- The characteristics of different parameters i.e. $V_{th}, DIBL$, SS, I_{on}, I_{off}, g_m has been studied by varying L, t_{si}, t_{ox} [41].The values are recorded and are compared with each other.

- To reduce further, the Graded channel engineering technique is used by varying the length of the channel and has beeen compared with the existing work without GCE [41]. It has been seen from the recorded value that the $DIBL$, SS, I_{off} reduces in GCE technique but SS for $L = 20nm.$, $10nm.$ becomes more than $70nm.$ Therefore this should be reduced. Further reduction of the parameters has been done by reducing the doping concentration of S/D region.

CHAPTER 5

Electrical Performance Optimization using MOGA

To optimize the electrical performance of the DG MOSFET, an optimization tool box MOGA of MATLAB is used. All the routines and programs for MOGA toolbox are developed using MATLAB 7.8 and all simulations are carried out on I5, 3.2GHz processor and 4GB RAM computer. For the implementation of the MOGA's tournament selection, which selects each parent by choosing individuals at random, is employed and then choosing the best individual out of that set to be a parent. Scattered crossover creates a random binary vector. Then, it selects the genes where the vector is a unity from the first parent and the genes where the vector is zero from the second parent and combines the genes to form the child. An optimization process is performed for a population size of 20 and a maximum number of generations equal to 100, for which the stabilization of the fitness function is obtained. In this chapter, Four objective functions are considered, i.e. Threshold voltage roll-off, Drain Induced Barrier Lowering (DIBL), Subthreshold swing (SS), Velocity saturation.

5.1 Introduction

The objective of this chapter is to optimize the objective function using simple MOGA toolbox. The objectives are generally conflicting, preventing simultaneous optimization of each objective. Many, or even most, real engineering problems actually do have multiple objectives, i.e., minimize cost, maximize performance, maximize reliability, etc. These are difficult but realistic problems. GA is a popular meta-heuristic that is particularly well-suited for this class of problems. Traditional Genetic Algorithm (GA) is customized to accommodate multi-objective problems by using specialized fitness functions and introducing methods to promote solution diversity. This can be rather arbitrary. In both cases, an optimization method would return a single solution rather than a set of solutions that can be examined for trade-offs. For this reason, decision-makers often prefer a set of good solutions considering the multiple objectives.

This approach is to determine an entire Pareto optimal solution set or a representative subset. A Pareto optimal set is a set of solutions that are non-dominated with respect to each other. While moving from one Pareto solution to another, there is always a certain amount of sacrifice in one objective(s) to achieve a certain amount of gain in the other(s). Pareto optimal solution sets are often preferred to single solutions because they can be practical when considering real-life problems since the final solution of the decision-maker is always a trade-off. Pareto optimal sets can be of varied sizes, but the size of the Pareto set usually increases with the increase in the number of objectives.

In mathematical programming, an objective is a function that we seek to optimize, via changes in the problem variables.

5.2 Multi-objective optimization

Multi-objective optimization (or multi-objective programming) is the process of simultaneously optimizing two or more conflicting objectives subjected to certain constraints or Multi-objective Optimization (MO) problems are defined as those problems, where two or more, sometimes competing and/or incommensurable, objective functions have to be minimized simultaneously. Multi objective optimization problems can be found in various fields: product and process design, finance, aircraft design, the oil and gas industry, automobile design, or wherever optimal decisions need to be taken in the presence of trade-offs between two or more conflicting objectives. Maximizing profit and minimizing the cost of a product, maximizing performance and minimizing fuel consumption of a vehicle and minimizing weight

while maximizing the strength of a particular component are examples of multi-objective optimization problems. For nontrivial multi objective problems, one cannot identify a single solution that simultaneously optimizes each objective. While searching for solutions, one reaches points such that, when attempting to improve an objective further, other objectives suffer as a result. A tentative solution is called non-dominated, Pareto optimal, or Pareto efficient if it cannot be eliminated from consideration by replacing it with another solution which improves an objective without worsening another one. Finding such non-dominated solutions, and quantifying the trade-offs in satisfying the different objectives, is the goal when setting up and solving a multi objective optimization problem. In a general case, the solution to the Multi objective problem is a set of points that represent the best trade-offs between the objective functions. These points are called Pareto Optimal points. The set of all the Pareto Optimal points is called the Pareto Optimal Set. A point in the search space is Pareto Optimal, if it is not pareto-dominated by any other point.

5.2.1 Multi-objective optimization formulation

Multi-objective formulations are realistic models for many complex engineering optimization problems. In many real-life problems, objectives under consideration conflict with each other, and optimizing a particular solution with respect to a single objective. A reasonable solution to a multi-objective problem is to investigate a set of solutions, each of which satisfies the objectives at an acceptable level without being dominated by any introducing methods to promote solution diversity. A minimization multi-objective decision problem with K objectives is defined as follows: Given an n-dimensional decision variable vector $x = \{x_1, ..., x_n\}$ in the solution space X, find a vector x^* that minimizes a given set of K objective functions $z(x^*) = \{z_1(x^*), ..., z_n(x^*)\}$. The solution space X is generally restricted by a series of constraints, such as $g_j(x^*) = b_j$ for j $= 1, \ldots, $ m and bounds on the decision variables. In many real-life problems, objectives under consideration conflict with each other. Hence, optimizing x with respect to a single objective often results in unacceptable results with respect to the other objectives. Therefore, a perfect multi-objective solution that simultaneously optimizes each objective function is almost impossible. A reasonable solution to a multi-objective problem is to investigate a set of solutions, each of which satisfies the objectives at an acceptable level without being dominated by any other solution.

If all objective functions are for minimization, a feasible solution x is said to dominate another feasible solution y ($x > y$), if and only if, $z_i(x) <= z_i(y)$ for i $= 1, \ldots, $ K and

$z_j(x) < z_j(y)$ for at least one objective function j. A solution is said to be Pareto optimal if it is not dominated by any other solution in the solution space. A Pareto optimal solution cannot be improved with respect to any objective without worsening at least one other objective. The set of all feasible non-dominated solutions in X is referred to as the Pareto optimal set, and for a given Pareto optimal set , the corresponding objective function values in the objective space are called the Pareto front. The ultimate goal of a multi-objective optimization algorithm is to identify solutions in the Pareto optimal set. In addition, for many problems, especially for combinatorial optimization problems, proof of solution optimality is computationally infeasible. Therefore, a practical approach to multi-objective optimization is required to investigate a set of solutions (the best-known Pareto set) that represent the Pareto optimal set as well as possible. With these concerns in mind, a multi-objective optimization approach should achieve the following three conflicting goals.

1. The best-known Pareto front should be as close as possible to the true Pareto front. Ideally, the best-known Pareto set should be a subset of the Pareto optimal set.

2. Solutions in the best-known Pareto set should be uniformly distributed and diverse over the Pareto front in order to provide the decision-maker a true picture of trade-offs.

3. The best-known Pareto front should capture the whole spectrum of the Pareto front. This requires investigating solutions at the extreme ends of the objective function space. For a given computational time limit, the first goal is best served by focusing (intensifying) the search on a particular region of the Pareto front. On the contrary, the second goal demands the search effort to be uniformly distributed over the Pareto front. The third goal aims at extending the Pareto front at both the ends, exploring new extreme solutions. This thesis presents common approaches used in multiobjective GA to attain these three conflicting goals while solving a multi-objective optimization problem.

5.3 Genetic Algorithm

The concept of GA was developed by Holland and his colleagues in the 1960s and 1970s. GA is inspired by the evolutionary theory explaining the origin of species. In nature, weak and unfit species within their environment faces extinction by natural selection. The strong ones have greater opportunity to pass their genes to future generations via reproduction. In the long run, species carrying the correct combination in their genes become dominant in their

population. Sometimes, during the slow process of evolution, random changes may occur in genes. If these changes provide additional advantages in the challenge for survival, new species evolve from the old ones. Unsuccessful changes are eliminated by natural selection. In GA terminology, a solution vector x $\in$ X is called an individual or a chromosome. Chromosomes are made of discrete units called genes. Each gene controls one or more features of the chromosome. In the original implementation of GA by Holland, genes are assumed to be binary digits. In later implementations, more varied gene types have been introduced. Normally, a chromosome corresponds to a unique solution x in the solution space. This requires a mapping mechanism between the solution space and the chromosomes. This mapping is called an encoding. In fact, GA work on the encoding of a problem, not on the problem itself.

GA operate with a collection of chromosomes which is called population. The population is normally initialized randomly. GA uses two operators to generate new solutions from existing ones: crossover and mutation. The crossover operator is the most important operator of GA. In crossover, generally two chromosomes, called parents, are combined together to form new chromosomes, called offspring. The parents are selected among existing chromosomes in the population with preference towards fitness so that offspring is expected to inherit good genes which make the parents fitter. By iteratively applying the crossover operator, genes of good chromosomes are expected to appear more frequently in the population, eventually leading to convergence to an overall good solution. The mutation operator introduces random changes into characteristics of chromosomes. Mutation is generally applied at the gene level. In typical GA implementations, the mutation rate (probability of changing the properties of a gene) is very small and depends on the length of the chromosome. Therefore, the new chromosome produced by mutation will not be different from the original one. Mutation plays a critical role in GA. As discussed earlier, crossover leads the population to converge by making the chromosomes in the population alike. Mutation re-introduces genetic diversity back into the population and assists the search escape from local optima. Reproduction involves selection of chromosomes for the next generation. In the most general case, the fitness of an individual determines the probability of its survival for the next generation. There are different selection procedures in GA depending on how the fitness values are used. Proportional selection, ranking, and tournament selection are the most popular selection procedures. The procedure of a generic GA is given as follows:

Step 1: Set $t = 1$. Randomly generate N solutions to form the first population, P_1. Evaluate the fitness of solutions in P1.

Step 2: Crossover: Generate an offspring population Q_t as follows:

1. Choose two solutions x and y from P_t based on the fitness values.
2. Using a crossover operator, generate offspring and add them to Q_t.

Step 3: Mutation: Mutate each solution x $\in Q_t$ with a predefined mutation rate.

Step 4: Fitness assignment: Evaluate and assign a fitness value to each solution x $\in Q_t$ based on its objective function value and infeasibility.

Step 5: Selection: Select N solutions from Q_t based on their fitness and copy them to $P_t + 1$

Step 6: If the stopping criterion is satisfied, terminate the search and return to the current population, else, set $t = t + 1$ go to Step 2.

5.4 Multi-objective Genetic Algorithm

Being a population-based approach, GA is well suited to solve multi-objective optimization problems. A generic single-objective GA can be modified to find a set of multiple non-dominated solutions in a single run. The ability of GA to simultaneously search different regions of a solution space makes it possible to find a diverse set of solutions for difficult problems with non-convex, discontinuous and multi-modal solutions spaces. The crossover operator of GA may exploit structures of good solutions with respect to different objectives to create new non dominated solutions in unexplored parts of the Pareto front. In addition, most multi-objective GA do not require the user to prioritize, scale, or weigh objectives. Therefore, GA have been the most popular heuristic approach to multi-objective design and optimization problems. Jones et al. [43] reported that 90 percent of the approaches to multi objective optimization aimed to approximate the true Pareto front for the underlying problem. A majority of these used a meta-heuristic technique, and 70 percent of all meta heuristics approaches were based on evolutionary approaches. The first multi objective GA, called vector evaluated GA (or VEGA) [38], was proposed by Schaffer. Afterwards, several multi-objective evolutionary algorithms were developed including Multi-objective Genetic Algorithm (MOGA) [42], Niched Pareto Genetic Algorithm (NPGA), Weight-based Genetic Algorithm (WBGA), Random Weighted Genetic Algorithm (RWGA), Non dominated Sorting Genetic Algorithm (NSGA), Strength Pareto Evolutionary Algorithm (SPEA), Pareto-Archived Evolution Strategy (PAES), Pareto Envelope-based Selection Algorithm (PESA),

Region-based Selection in Evolutionary Multi objective Optimization (PESA-II), Fast Non-dominated Sorting Genetic Algorithm (NSGA-II), Multi-objective Evolutionary Algorithm (MEA), Micro-GA, Rank-Density Based Genetic Algorithm (RDGA) and Dynamic Multi-objective Evolutionary Algorithm (DMOEA). Generally, multi-objective GA differs based on their fitness assignment procedure, elitism, or diversification approaches. However, the discussion in this thesis is aimed at introducing the components of multi-objective GA to researchers without a background on the multi-objective GA. Multi objective optimization is concerned with the minimization of multiple objective functions that are subject to a set of constraints. The multi objective genetic algorithm solver is used to solve multi objective optimization problems by identifying the Pareto front-the set of evenly distributed non dominated optimal solutions. We can use this solver to solve smooth or non smooth optimization problems with or without bound and linear constraints. The multi objective genetic algorithm does not require the functions to be differentiable or continuous. The Optimization Toolbox specifies:

- Population size
- Crossover fraction
- Pareto fraction
- Distance measure across individuals
- Migration among sub-populations (using ring topology)
- Linear and bound constraints for an optimization problem

The algorithm can be customized options by providing user-defined functions and represent the problem in a variety of data formats, for example by defining variables that are integers, mixed integers, categorical, or complex. We can base the stopping criteria for the algorithm on time, fitness limit, or number of generations.

5.5 Performance enhancement by using MOGA

This segment of the Thesis considers four objective functions to be optimized which are already discussed in chapters 1, 2, 3 and 4. These objective functions are Threshold voltage roll-off, SS, DIBL and velocity saturation. These objective functions can only be optimized by searching the proper design variables or input variables which are Thickness of silicon

layer, Thickness of the oxide layer, Length of the channel, Gate voltage and Drain voltage. The optimization of the objective function can be done by optimization toolbox i.e. MOGA, which is a very user friendly tool for Multi-objective optimization. In the lower subsection, a detail procedure to handle this toolbox is explained briefly in stepwise manner.

5.5.1 Objective

- To minimize Threshold voltage roll-off
- To minimize Sub-threshold swing
- To minimize DIBL
- To minimize Velocity Saturation

5.5.2 Input Variables (X)

$X = \begin{bmatrix} t_{si} & t_{ox} & L & V_g & V_{ds} \end{bmatrix}$

5.5.3 Procedure

The MOGA computation has been done by using MATLAB 7.8 toolbox. Using MOGA toolbox, the electrical parameters such as Threshold voltage roll-off, Sub-threshold swing, DIBL and Velocity saturation have been minimized by considering five variables like $t_{si}, t_{ox}, L, V_g, V_d$

Step 1
- Go to the Start button of MATLAB (command window).
- $Start \rightarrow ToolBoxes \rightarrow Optimization \rightarrow Optimizationtool(Optimtool)$

Step 2
- Solver: In the optimization tool window, go to the left topmost of the window (Problem setup and results) , to set the solver to gamultiobj → Multi-objective optimization using Genetic Algorithm.
- Fitness function: Write the user defined function for the optimization in the fitness function box. Fitness function is the multiobjective (vector function) function that is to be minimized. The function can be specified of the form mymultidgmosfet3, where mymultidgmosfet3.m is an M-file, that returns a vector (Objective functions). In our case four objective functions are $f(1)$ for Threshold voltage roll-off, $f(2)$ for DIBL, $f(3)$ for Threshold swing, $f(4)$ for Velocity saturation.
- Number of variables: It is the number of independent variables for the fitness function . In our case, five number of variables are set which are $X = \begin{bmatrix} t_{si} & t_{ox} & L & V_g & V_d \end{bmatrix}$.

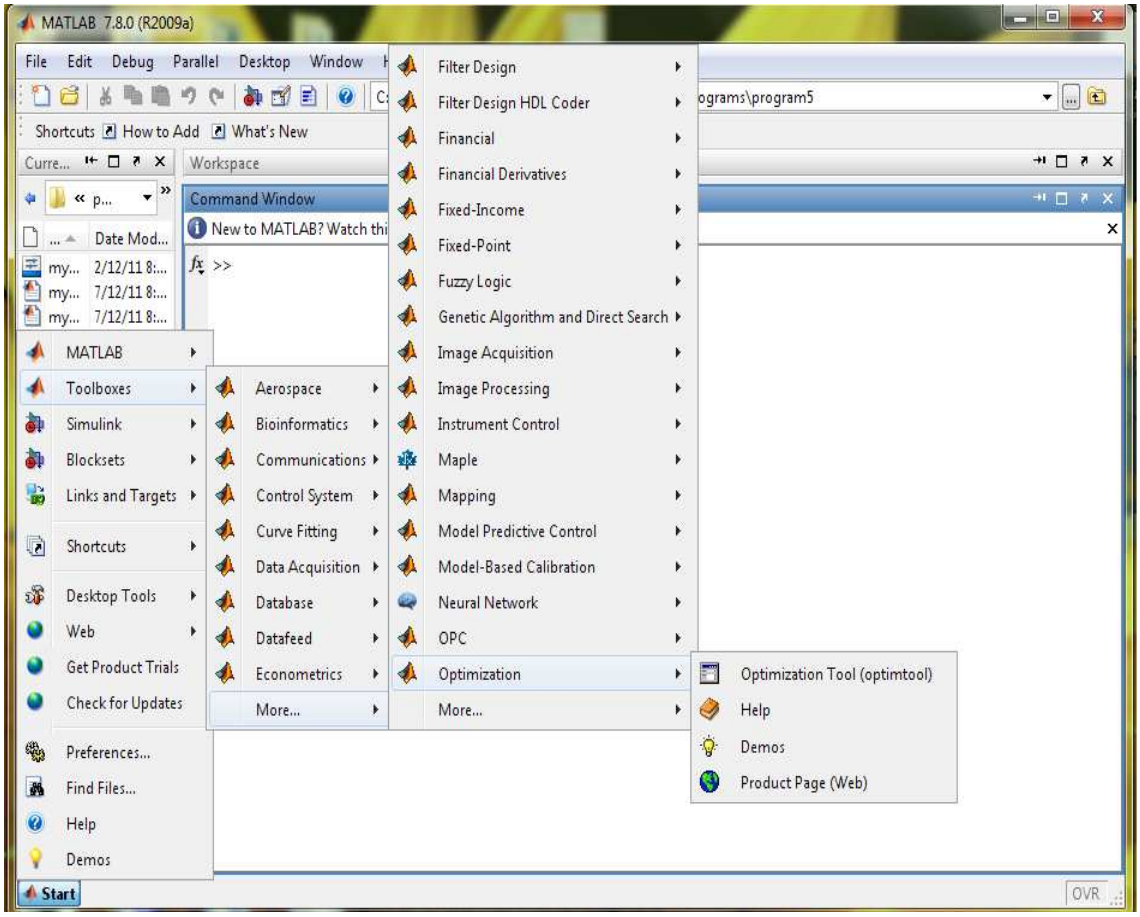

Figure 5.1: The Optimization toolbox diagram

- Constraints: In constraints only bounds (boundary conditions) are set. Lower specifies lower bounds and upper specifies upper bounds of a function.

Step 3

- Population: In option part, Population options specify options for the population of the genetic algorithm. Population type specifies the type of the input to the fitness function. Population type can be set to be Double vector, or Bit string, or Custom. Here population type is Double vector. Population size specifies how many individuals are in each generation. In this case the population size has been taken as 20.
- Selection: The selection function chooses parents for the next generation based on their scaled values from the fitness functions. The selection function can be of two types. Tournament selects each parent by choosing individuals at random, the number of which you can specify by Tournament size, and then choosing the

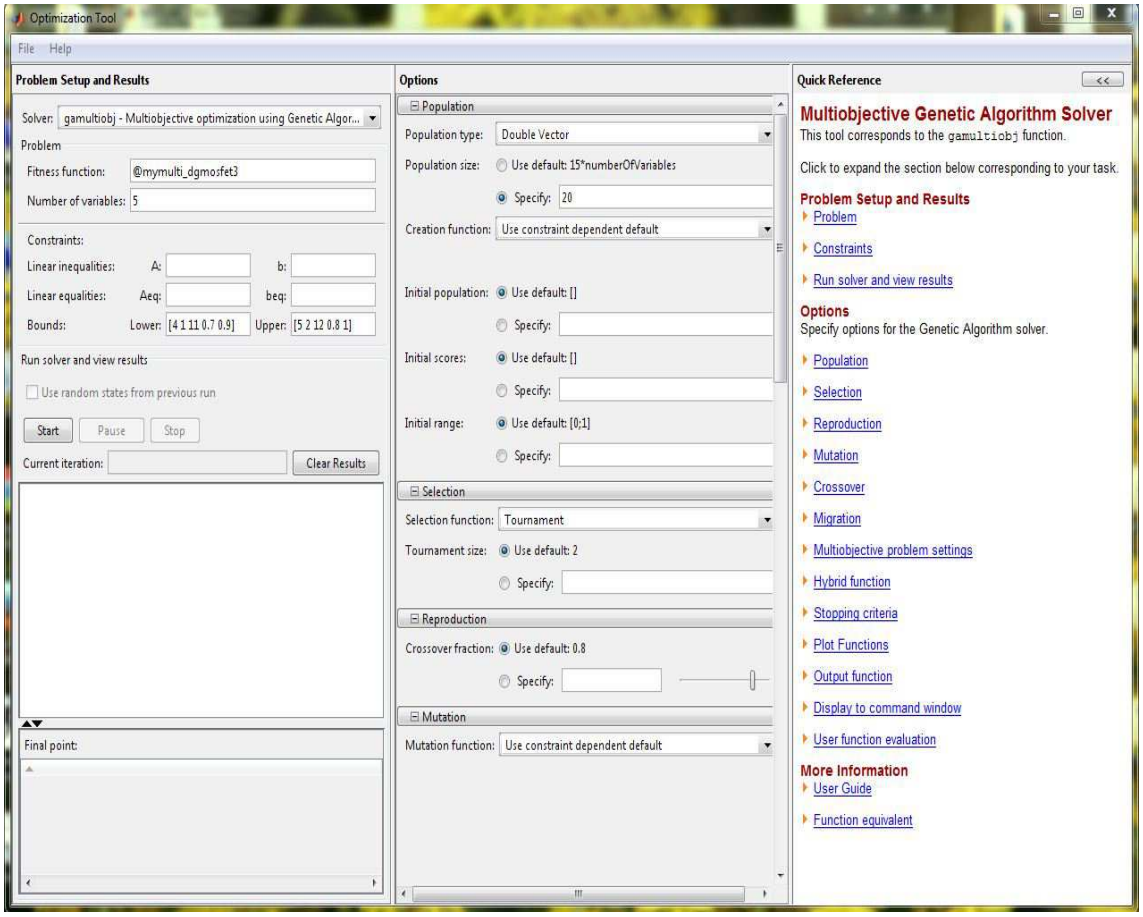

Figure 5.2: The Multi-objective optimization toolbox diagram

best individual out of that set to be a parent. Custom enables you to write your own selection function. Here the selection function has been taken as Tournament and the Tournament size has been taken as 2.

Step 4 Click the start button of run solver and view results.

5.6 Result Analysis

The MOGA is an user friendly optimization toolbox which is used to optimize the electrical performances by changing five variables $(t_{ox}, t_{si}, L, V_g, V_d)$, which are the design parameters of the DG-MOSFET.

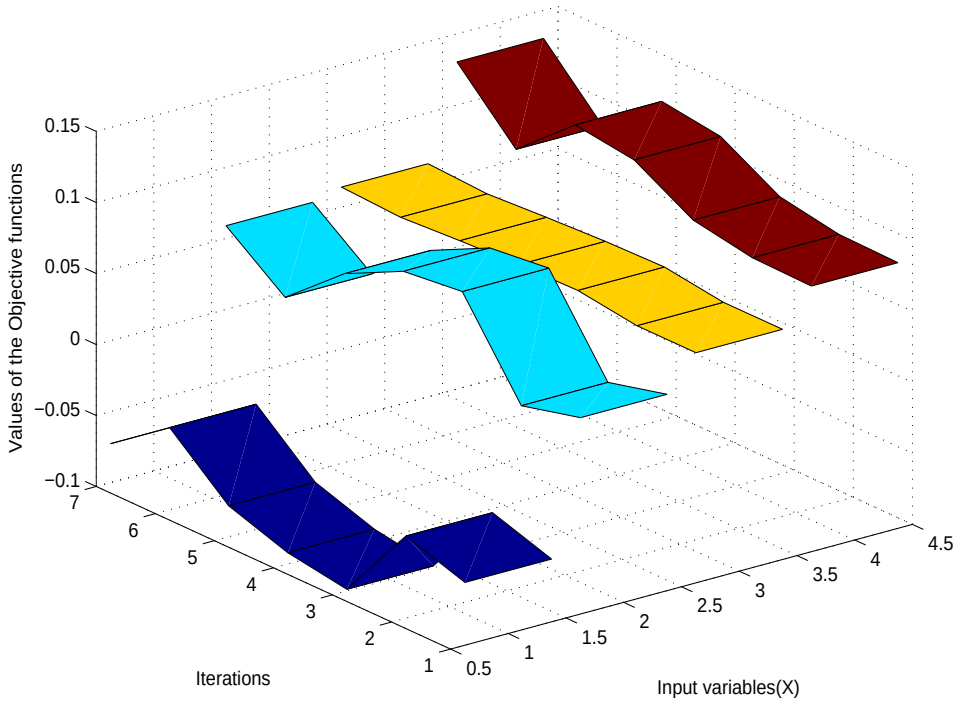

Figure 5.3: The variation of objective function w.r.t input variable

By following the steps mentioned in the above section, it is easy to handle multi-objective optimization by this Toolbox. From the optimization, the Threshold voltage roll-off (ΔV_{th}) is optimized to -0.105 V, SS to 0.063 V/decade, DIBL to 0.192 V/V and V_{sat} to 0.132 m/s with the designed parameters t_{si}=4.7nm, t_{ox}=1 nm, L=10 nm, V_g= 0.78 V and V_d= 0.85 V. This result is compared to a existing result [32]. The structure with these design parameters reduces the SCEs as a result of which the performance enhances. To validate the structure, model has been built in ATLAS with these above design parameters. The Schematic diagram of the structure is shown in the Fig. 5.4. From the design structure, the SCEs are extracted and compared with the optimized results using MOGA technique which given in Table 5.1. The simulation result found is nearly same as the optimized result found by MOGA technique. This validates our design Model. From, the comparison shown in the Table 5.1, also it is clearly viewed that our proposed technique for reduction of SCEs is better than the existing technique for designing purpose.

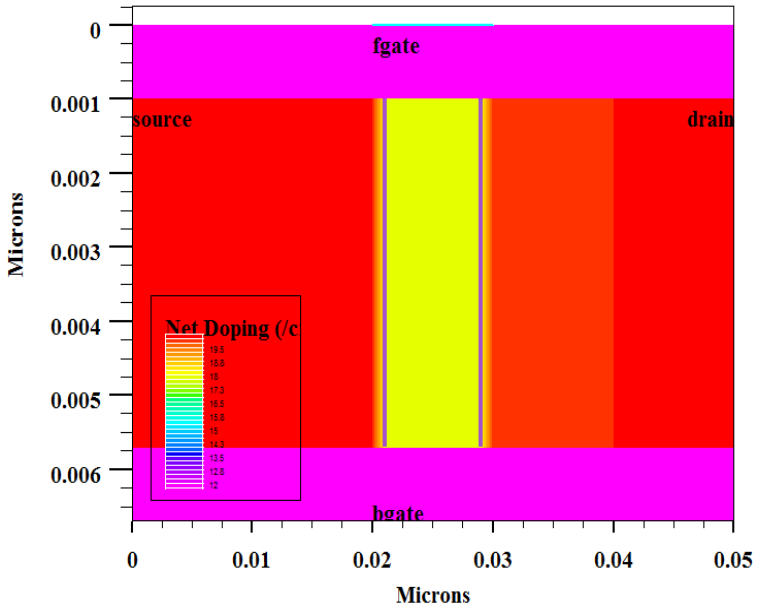

Figure 5.4: Schematic Diagram of DG MOSFET using optimized parameter

Table 5.1: Table for comparison of electrical performances

Symbol	Quantity	Existing design[32]	Simulated results with GCE	Optimized design	Simulated results with optimised parameters
t_{si}	Silicon thickness	5 nm	5 nm	4.7	4.7 nm
t_{ox}	Oxide thickness	1 nm	1 nm	1 nm	1 nm
L	Channel Length	10 nm	10 nm	10 nm	10 nm
V_g	Gate Voltage	0.9 V	0.9 V	0.78 V	0.78 V
V_d	Drain Voltage	0.8 V	0.8 V	0.85 V	0.85 V
ΔV_{th}	Threshold voltage roll-off	-0.201 V	-0.183 V	-0.105 V	-0.1045 V
SS	Threshold swing	0.092 V/decade	0.068 V/decade	0.063 V/decade	0.0632 V/decade
$DIBL$	Drain Induced Barrier lowering	0.864 V/V	0.4775 V/V	0.192 V/V	0.1899 V/V
ν_{sat}	Velocity saturation	0.092 m/s	0.1002 m/s	0.1320 m/s	0.1342 m/s

5.7 Summary

- In this chapter, a MOGA based approach is used to optimize the electrical performance of DG MOSFET has been proposed. The aim of the use of MOGA is to optimize the electrical performance of short channel effects of the nanoscale DG MOSFETs.
- This approach has successfully searched the design parameters for which electrical performances has been improved.
- The present result has been compared with the existing result[32] and also with the results obtained by the structure obtained by the structure ,with GCE with $N_D = N_S = 0.5e20cm^{-3}$ doping concentration .It has been shown that the MOGA based searching approach gives the optimum performances with suitable bounded input design parameters.

CHAPTER 6

Conclusion and Future Scope

6.1 Conclusion of the thesis

Starting with review of CMOS scaling, this thesis focuses on different analytical modeling and optimization of the short channel effects of DG MOSFETs. The 1-dimensional analytical modeling shows the band bending which is totally dependent on charge density and gate voltage. The current modeling gives the expression of velocity saturation for DG MOSFET. Then, a threshold modeling has been studied to derive the expression of short channel effects like sub threshold swing, threshold voltage roll-off and DIBL. It has been seen that the SS, DIBL increases and threshold voltage roll-off decreases with decreasing channel length of DG MOSFET. To validate such models for SCEs, simulation has been done by using ATLAS device simulator. To reduce SCEs further a Graded Channel Engineering technique followed by change in doping concentration of S/D regime has been adopted. The results has been compared with the existing results without GCE and concluded that the results with GCE gives better performance. These features has also been controlled and optimized by MOGA optimization technique. The results of MOGA based optimization technique has also been compared with existing result. On the whole the thesis concluded that the MOGA based optimisation technique gives better results compared to other approaches.

6.2 Future Scopes

This thesis gives a new direction for research.

- A Multi-Objective Genetic Algorithm (MOGA) approach is adopted for optimizing the SCEs with some design parameters. Further, this thesis gives an indication that any other Multi-Objective Optimization techniques such Multi-Objective Particle Swarm optimization (MO-PSO), Multi-Objective Ant Colony Optimization (MO-ACO) techniques can be used for optimizing the SCEs and a comparative study may be done with MOGA.
- Different metal gates can be used like, Molybdenum(Mo), Tin metal in place of polysilicon gate material to reduce SCEs.
- Dual metal technology may be adopted to get better value of SCEs.

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